Refine Search

Search Results -

Terms	Documents
L3	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 14, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT; PLUR=YES; OP=OR			
L3	l2 and ((module or device or unit) same (connector near10 cable))	20	L3
L2	L1 same control$4	99	L2
L1	(module or device or unit) same (connector near10 pin) same (respon$4 near5 signal)	169	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L2 and ((module or device or unit) same (connector near10 cable))	20

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 14, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L3	l2 and ((module or device or unit) same (connector near10 cable))	20	L3
L2	L1 same control$4	99	L2
L1	(module or device or unit) same (connector near10 pin) same (respon$4 near5 signal)	169	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(439/189 |439/497 |439/502 |439/620 |439/505 |174/34 |709/253 |710/3 |710/100 |710/300 |710/305 |710/301 |710/316 |710/1 |710/313 |710/72 |710/63 |340/825.52 |235/462.15 |235/361 |714/25).ccls.	8319

Database:
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- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, May 17, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L1	710/3,100,300,305,301,316,1,313,72,63;439/189,497,502,620,505;235/462.15,361/683,686,752,7

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and L3	21

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, May 17, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L4	l1 and L3
L3	(module or device or unit) same (connector near10 pin) same (respon$4 near5 signal)
L2	(module or device or unit) same (connector near10 pin) same (respon$4 nera5 signal)
L1	710/3,100,300,305,301,316,1,313,72,63;439/189,497,502,620,505;235/462.15,361/683,686,752,7

END OF SEARCH HISTORY

h e b b cg b e e ch

WEST

Generate Collection | Print

L1: Entry 1 of 5 File: USPT Aug 17, 1999

US-PAT-NO: 5938754
DOCUMENT-IDENTIFIER: US 5938754 A

TITLE: Fieldbus connector including dual connectors

DATE-ISSUED: August 17, 1999

INT-CL: [6] G06 F 13/00

US-CL-ISSUED: 710/129; 714/27
US-CL-CURRENT: 710/305; 714/27

FIELD-OF-SEARCH: 395/183.03, 395/183.21, 395/200.54, 395/280, 395/306, 395/309, 439/255, 714/27, 714/45, 710/100, 710/126, 710/129, 709/224

WEST

Generate Collection | Print

L1: Entry 2 of 5 File: USPT May 18, 1999

US-PAT-NO: 5905249
DOCUMENT-IDENTIFIER: US 5905249 A

TITLE: Multiple-interface selection system for computer peripherals

DATE-ISSUED: May 18, 1999

INT-CL: [6] G06 K 7/10

US-CL-ISSUED: 235/462.15; 235/462.13, 235/462.43
US-CL-CURRENT: 235/462.15; 235/462.13, 235/462.43

FIELD-OF-SEARCH: 235/462, 235/472, 235/462.15, 235/462.13, 235/462.43, 235/462.45, 235/462.47, 439/502, 439/620

WEST

Generate Collection | Print

L1: Entry 3 of 5 File: USPT Dec 30, 1997

US-PAT-NO: 5703347
DOCUMENT-IDENTIFIER: US 5703347 A

TITLE: Multiple-interface selection system for computer peripherals

DATE-ISSUED: December 30, 1997

INT-CL: [6] G06 K 7/10

US-CL-ISSUED: 235/472; 235/462
US-CL-CURRENT: 235/462.15

FIELD-OF-SEARCH: 235/462, 235/472, 235/436, 439/329, 439/488, 439/489, 439/491, 439/620, 439/502

WEST

Generate Collection | Print

L1: Entry 4 of 5 File: USPT Dec 9, 1997

US-PAT-NO: 5696988
DOCUMENT-IDENTIFIER: US 5696988 A

TITLE: Current/voltage configurable I/O module having two D/A converters serially coupled together such that data stream flows through the first D/A to the second D/A

DATE-ISSUED: December 9, 1997

INT-CL: [6] G06 F 13/12

US-CL-ISSUED: 395/821; 395/824, 341/144, 341/139
US-CL-CURRENT: 710/1; 341/139, 341/144, 710/4

FIELD-OF-SEARCH: 340/347, 341/145, 341/139, 341/144, 364/900, 360/31, 324/248, 395/821, 395/824

WEST

End of Result Set

☐ Generate Collection Print

L1: Entry 5 of 5 File: USPT Jan 21, 1997

US-PAT-NO: 5596169
DOCUMENT-IDENTIFIER: US 5596169 A

TITLE: Combined SCSI/parallel port cable

DATE-ISSUED: January 21, 1997

INT-CL: [6] H01 B 11/02

US-CL-ISSUED: 174/33; 174/34, 341/89, 439/505
US-CL-CURRENT: 174/33; 174/34, 341/89, 439/502, 439/505

FIELD-OF-SEARCH: 174/33, 174/27, 174/32, 174/34, 361/686, 439/65, 341/89, 341/100, 341/101

Most Frequently Occurring Classifications of Patents Returned
From A Search of 10071870 on May 28, 2003

Original Classifications

5	439/76.1
4	385/24
3	361/119
3	361/686
3	439/215
2	174/48
2	324/537
2	361/624
2	375/257
2	439/535
2	439/709

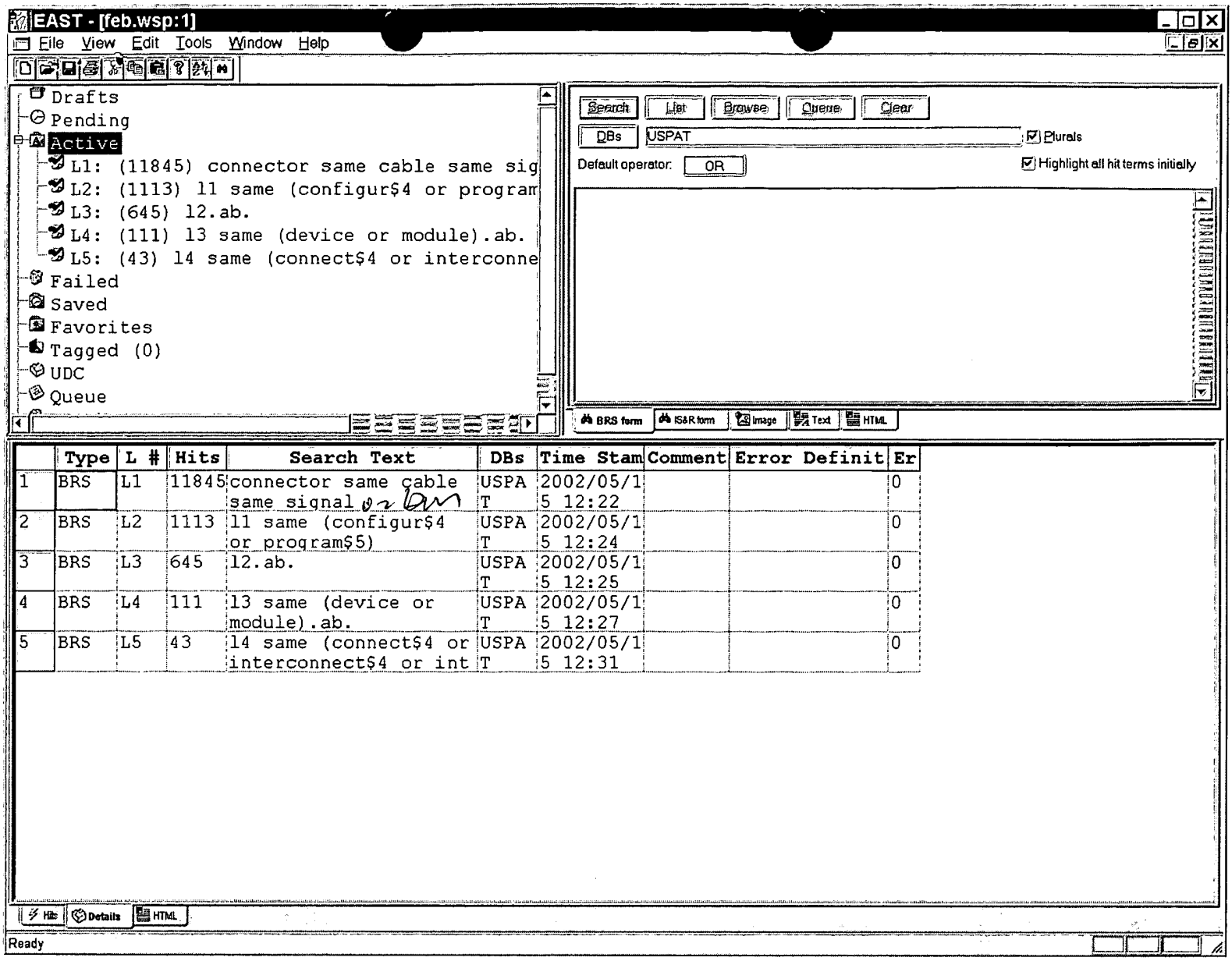
Cross-Reference Classifications

4	361/683
4	385/17
4	439/225
3	174/58
3	385/23
3	385/88
3	439/502
2	174/53
2	174/59
2	257/E23.172
2	361/119
2	361/626
2	361/715
2	361/725
2	361/730
2	361/735
2	361/736
2	361/748
2	361/785
2	361/796
2	361/823
2	361/824
2	370/254
2	375/219
2	379/25
2	385/89
2	398/161
2	439/49
2	439/535
2	439/540.1
2	439/61
2	439/638
2	439/77

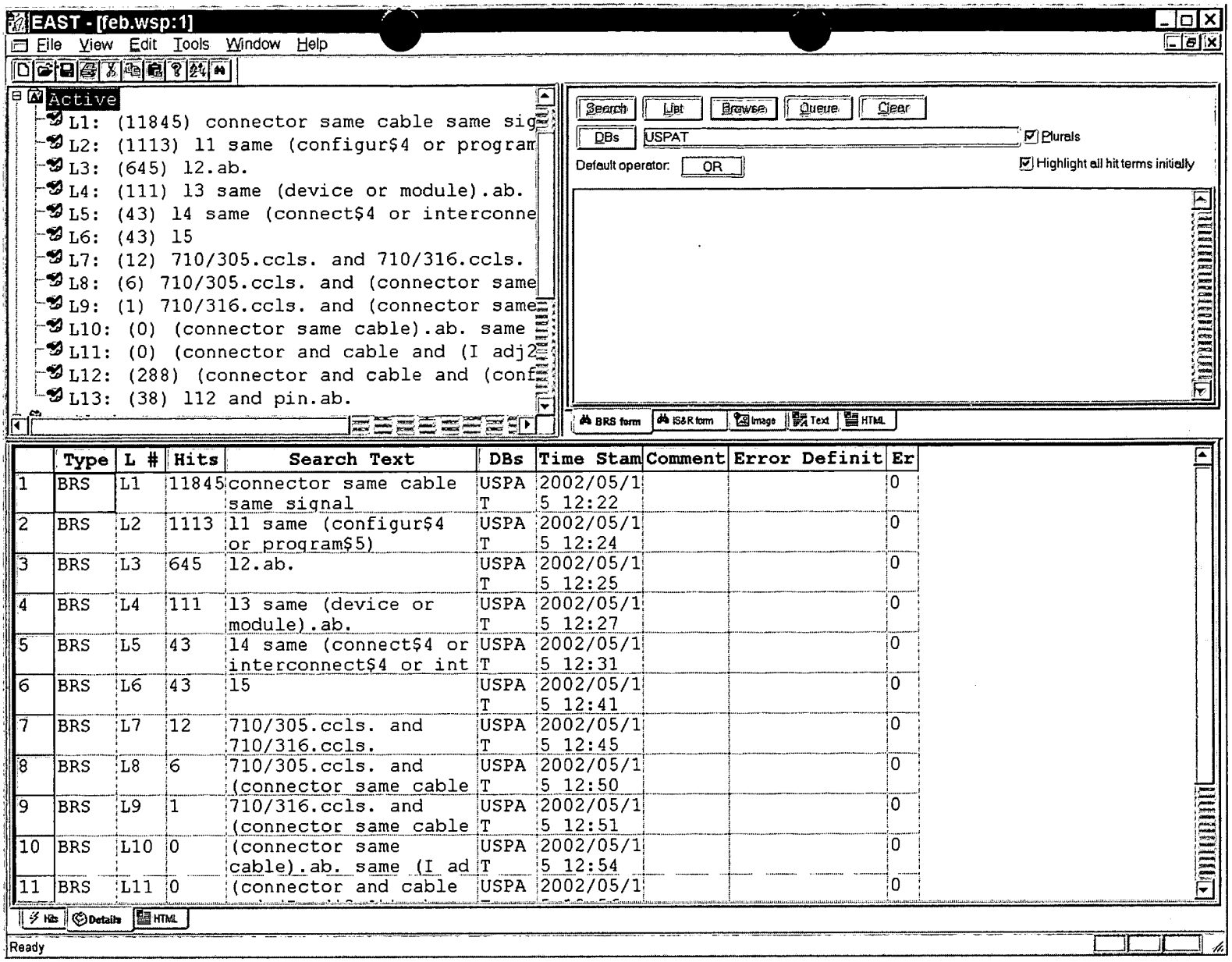
Combined Classifications

5	361/119
5	385/24
5	439/76.1
4	361/683

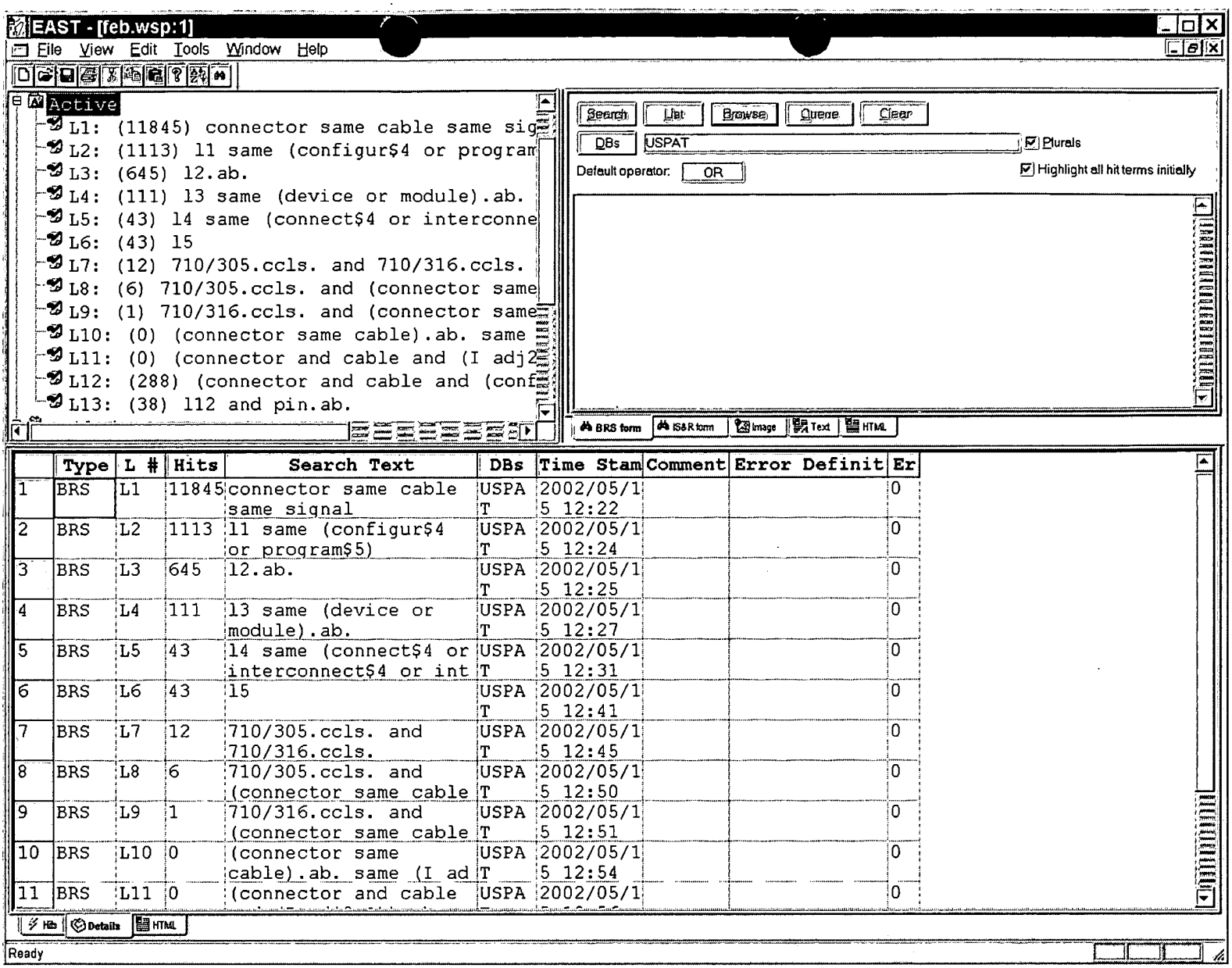
4	361/686
4	385/17
4	439/225
4	439/535
3	174/58
3	361/624
3	361/735
3	361/796
3	375/257
3	379/25
3	385/23
3	385/88
3	385/89
3	439/215
3	439/49
3	439/502
2	174/48
2	174/53
2	174/59
2	220/3.3
2	257/E23.172
2	324/537
2	324/539
2	361/626
2	361/715
2	361/725
2	361/730
2	361/736
2	361/748
2	361/785
2	361/823
2	361/824
2	370/254
2	370/445
2	370/465
2	375/219
2	379/331
2	385/135
2	385/76
2	385/92
2	398/161
2	439/347
2	439/540.1
2	439/61
2	439/63
2	439/638
2	439/709
2	439/77
2	439/92
2	710/100
2	710/316
2	710/72



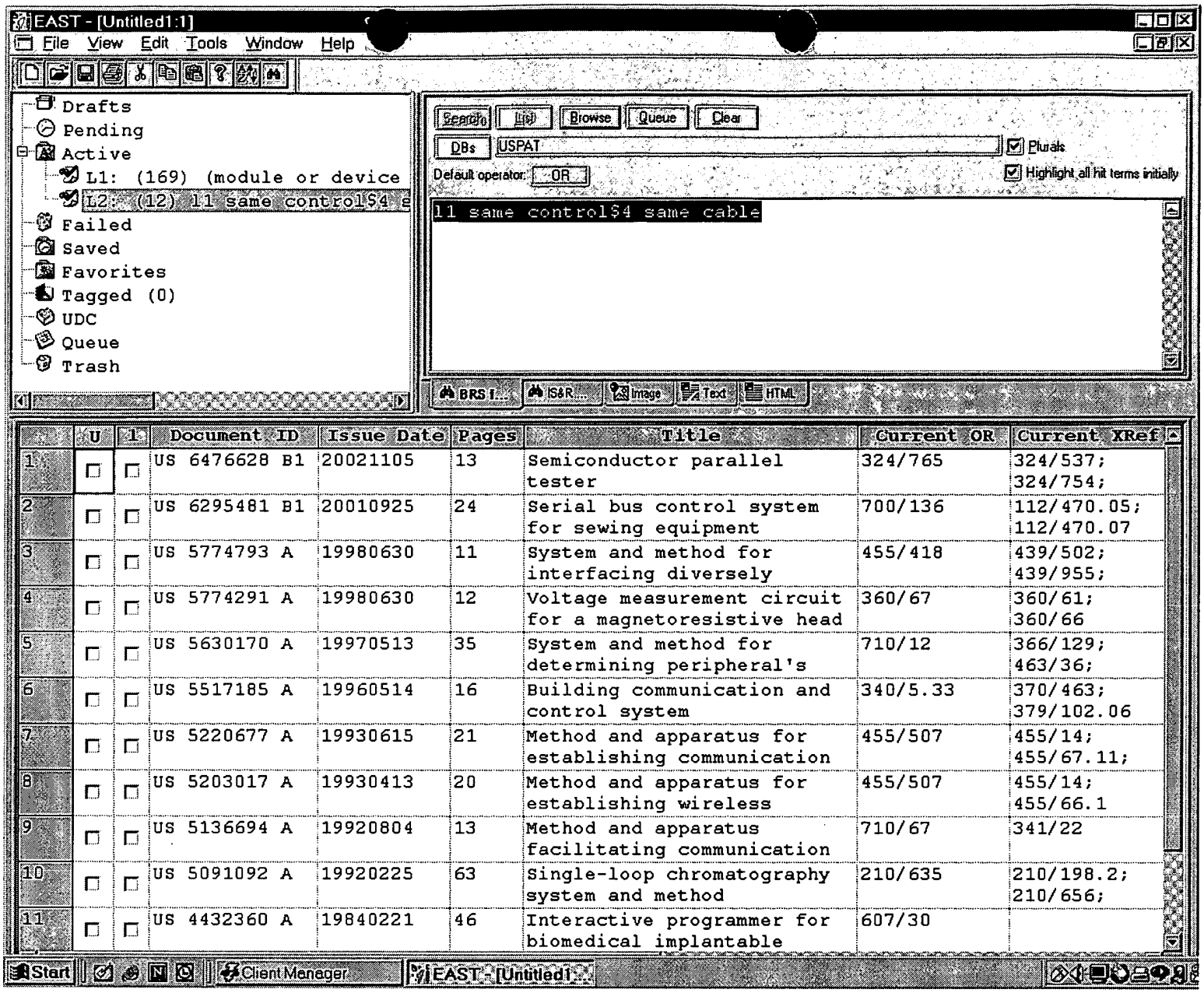
	Type	L #	Hits	Search Text	DBs	Time Stam	Comment	Error Definit	Er
1	BRS	L1	11845	connector same cable same signal	USPAT	2002/05/15 12:22			0
2	BRS	L2	1113	l1 same (configur$4 or program$5)	USPAT	2002/05/15 12:24			0
3	BRS	L3	645	l2.ab.	USPAT	2002/05/15 12:25			0
4	BRS	L4	111	l3 same (device or module).ab.	USPAT	2002/05/15 12:27			0
5	BRS	L5	43	l4 same (connect$4 or interconnect$4 or int	USPAT	2002/05/15 12:31			0



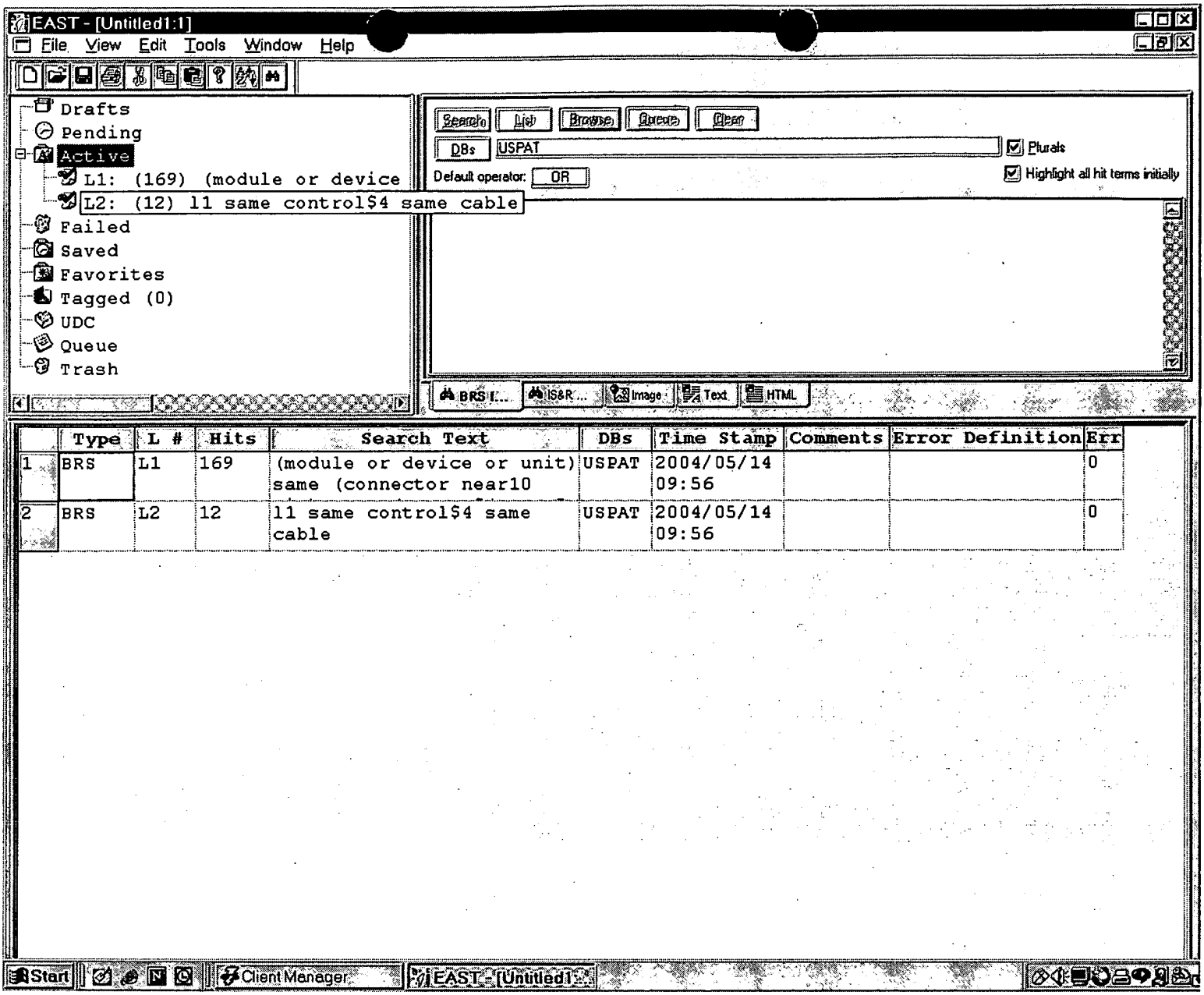
	Type	L #	Hits	Search Text	DBs	Time Stam	Comment	Error Definit	Er
1	BRS	L1	11845	connector same cable same signal	USPAT	2002/05/15 12:22			0
2	BRS	L2	1113	l1 same (configur$4 or program$5)	USPAT	2002/05/15 12:24			0
3	BRS	L3	645	l2.ab.	USPAT	2002/05/15 12:25			0
4	BRS	L4	111	l3 same (device or module).ab.	USPAT	2002/05/15 12:27			0
5	BRS	L5	43	l4 same (connect$4 or interconnect$4 or int	USPAT	2002/05/15 12:31			0
6	BRS	L6	43	l5	USPAT	2002/05/15 12:41			0
7	BRS	L7	12	710/305.ccls. and 710/316.ccls.	USPAT	2002/05/15 12:45			0
8	BRS	L8	6	710/305.ccls. and (connector same cable	USPAT	2002/05/15 12:50			0
9	BRS	L9	1	710/316.ccls. and (connector same cable	USPAT	2002/05/15 12:51			0
10	BRS	L10	0	(connector same cable).ab. same (I ad	USPAT	2002/05/15 12:54			0
11	BRS	L11	0	(connector and cable	USPAT	2002/05/1			0



	Type	L #	Hits	Search Text	DBs	Time Stam	Comment	Error Definit	Er
1	BRS	L1	11845	connector same cable same signal	USPAT	2002/05/15 12:22			0
2	BRS	L2	1113	l1 same (configur$4 or program$5)	USPAT	2002/05/15 12:24			0
3	BRS	L3	645	l2.ab.	USPAT	2002/05/15 12:25			0
4	BRS	L4	111	l3 same (device or module).ab.	USPAT	2002/05/15 12:27			0
5	BRS	L5	43	l4 same (connect$4 or interconnect$4 or int	USPAT	2002/05/15 12:31			0
6	BRS	L6	43	l5	USPAT	2002/05/15 12:41			0
7	BRS	L7	12	710/305.ccls. and 710/316.ccls.	USPAT	2002/05/15 12:45			0
8	BRS	L8	6	710/305.ccls. and (connector same cable	USPAT	2002/05/15 12:50			0
9	BRS	L9	1	710/316.ccls. and (connector same cable	USPAT	2002/05/15 12:51			0
10	BRS	L10	0	(connector same cable).ab. same (I ad	USPAT	2002/05/15 12:54			0
11	BRS	L11	0	(connector and cable	USPAT	2002/05/1			0



	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6476628 B1	20021105	13	Semiconductor parallel tester	324/765	324/537; 324/754;
2	☐	☐	US 6295481 B1	20010925	24	Serial bus control system for sewing equipment	700/136	112/470.05; 112/470.07
3	☐	☐	US 5774793 A	19980630	11	System and method for interfacing diversely	455/418	439/502; 439/955;
4	☐	☐	US 5774291 A	19980630	12	Voltage measurement circuit for a magnetoresistive head	360/67	360/61; 360/66
5	☐	☐	US 5630170 A	19970513	35	System and method for determining peripheral's	710/12	366/129; 463/36;
6	☐	☐	US 5517185 A	19960514	16	Building communication and control system	340/5.33	370/463; 379/102.06
7	☐	☐	US 5220677 A	19930615	21	Method and apparatus for establishing communication	455/507	455/14; 455/67.11;
8	☐	☐	US 5203017 A	19930413	20	Method and apparatus for establishing wireless	455/507	455/14; 455/66.1
9	☐	☐	US 5136694 A	19920804	13	Method and apparatus facilitating communication	710/67	341/22
10	☐	☐	US 5091092 A	19920225	63	Single-loop chromatography system and method	210/635	210/198.2; 210/656;
11	☐	☐	US 4432360 A	19840221	46	Interactive programmer for biomedical implantable	607/30	



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	169	(module or device or unit) same (connector near10	USPAT	2004/05/14 09:56			0
2	BRS	L2	12	11 same control$4 same cable	USPAT	2004/05/14 09:56			0

US005774793A

United States Patent [19]

Cooper et al.

[11] Patent Number: 5,774,793

[45] Date of Patent: Jun. 30, 1998

[54] **SYSTEM AND METHOD FOR INTERFACING DIVERSELY CONTROLLED DEVICES TO A BUS CONNECTOR HAVING A COMMON SIGNAL FORMAT**

[75] Inventors: Gershon N. Cooper, Encino; Andrew Holman, West Hills, both of Calif.

[73] Assignee: ORA Electronics, Inc., Chatsworth, Calif.

[21] Appl. No.: 361,885

[22] Filed: Dec. 22, 1994

[51] Int. Cl.[6] H04B 1/38

[52] U.S. Cl. 455/89; 455/345; 455/127; 379/59; 439/502; 439/955

[58] Field of Search 455/89, 90, 127, 455/128, 344, 345, 346, 347, 348, 349, 350, 351, 33.1; 379/58, 59, 63, 441, 442; 439/502, 636, 505, 955

[56] References Cited

U.S. PATENT DOCUMENTS

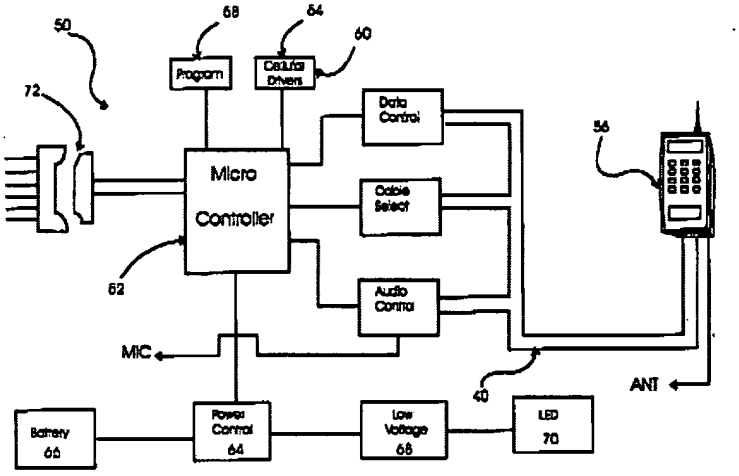
4,876,712	10/1989	Britz et al.	439/955
4,972,470	11/1990	Farago	439/935
5,249,218	9/1993	Sainton	379/58
5,333,177	7/1994	Bratberg et al.	379/58
5,418,835	5/1995	Yazaki	379/58
5,479,479	12/1995	Bratberg et al.	379/59

Primary Examiner—Reinhard J. Eisenzopf
Assistant Examiner—Doris To
Attorney, Agent, or Firm—Matthew F. Jodziewicz

[57] **ABSTRACT**

A system for connecting a plurality of cellular telephones, each responsive to device-specific command signals for its operation, to an automotive electronics and communications system through a bus connector having a known universal signal format, includes a docking station having a cradle member shaped for receiving at least one cellular telephone. An interface unit contains the hardware and firmware drivers necessary for controlling the selected cellular telephone. A user selected cable having a specific signal path configuration selects the needed drivers. A second cable connects the interface unit with the bus connector for communicating signals therebetween.

42 Claims, 4 Drawing Sheets



US005630170A

United States Patent [19]

Koizumi et al.

[11] Patent Number: 5,630,170

[45] Date of Patent: May 13, 1997

[54] **SYSTEM AND METHOD FOR DETERMINING PERIPHERAL'S COMMUNICATION MODE OVER ROW OF PINS DISPOSED IN A SOCKET CONNECTOR**

[75] Inventors: Masahiro Koizumi; Naoki Niizuma; Yasuhisa Kawase; Hajime Ikebe, all of Tokyo, Japan

[73] Assignee: Kabushiki Kaisha Sega Enterprises, Tokyo, Japan

[21] Appl. No.: 445,108

[22] Filed: May 19, 1995

[30] Foreign Application Priority Data

Oct. 12, 1994 [JP] Japan 6-246581

[51] Int. Cl.[6] G06F 3/00; G06F 3/023; G06F 13/38

[52] U.S. Cl. 395/834; 395/893; 463/36; 463/40

[58] Field of Search ..... 439/43, 189, 604, 439/45, 44, 46, 47, 49, 79, 95, 119, 221, 362, 369, 133; 395/834, 835, 831, 836, 893; 273/143 B; 463/36, 37, 38, 40; 345/161, 168

[56] References Cited

U.S. PATENT DOCUMENTS

4,484,266	11/1984	Becker et al.	364/200
4,501,424	2/1985	Stone et al.	273/143 B
4,592,012	5/1986	Brena	364/900
4,688,680	12/1989	Sandor et al.	364/200
4,972,470	11/1990	Farago	380/3
5,151,945	9/1992	Sandor et al.	395/500
5,175,820	12/1992	Gephardt	395/834
5,179,710	1/1993	Crochizi	395/750
5,207,426	5/1993	Inoue et al.	273/148 B
5,274,766	12/1993	Long et al.	595/834
5,375,210	12/1994	Monnes et al.	595/830
5,379,382	1/1995	Work et al.	395/275

FOREIGN PATENT DOCUMENTS

60-27566	2/1985	Japan .	
63-118830	5/1988	Japan .	
63-118928	5/1988	Japan .	
2-62518	3/1990	Japan .	
9110715	11/1992	United Kingdom .	
WO-A-8809573	12/1988	WIPO .	
WO-A-9416774	8/1994	WIPO .	
WO95/01609	1/1995	WIPO .	
WO95/01629	1/1995	WIPO .	
WO95/01630	1/1995	WIPO .	

OTHER PUBLICATIONS

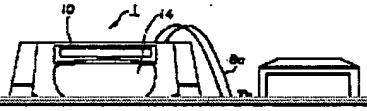
Patent Abstracts of Japan, vol. 14, No. 240, p. 151, May 22, 1990 (Abstract of JP 2-062618).

Primary Examiner—Thomas C. Lee
Assistant Examiner—D. Dinh
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] **ABSTRACT**

A peripheral device for use with a data processing apparatus. The apparatus has a peripheral port with a set of terminal pins consisting of first to ninth pins disposed in a row. The first pin is assigned for one of a power source and the ground potential, the ninth pin for the other of the power source and the ground potential, the second, third, seventh and eighth pins for transmitting data signals, and the fourth to sixth pins for transmitting control signals. The apparatus has an element for selecting the communication mode of the peripheral device connected to the peripheral port, based on the data signals transmitted from the second, third, seventh and eighth pins. The peripheral device comprises a plug connector detachably connected to the peripheral port, the plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row, a cable including a plurality of wires connecting the terminal pins of the plug connector with terminals on an internal printed circuit board, and an element for transmitting data signals including identification data representing the communication mode via at least one of the second, third, seventh and eighth pins in synchronization with a clock signal supplied from the apparatus.

61 Claims, 15 Drawing Sheets



US005938754A

United States Patent [19]

Edwards et al.

[11] Patent Number: 5,938,754

[45] Date of Patent: Aug. 17, 1999

[54] **FIELDBUS CONNECTOR INCLUDING DUAL CONNECTORS**

[75] Inventors: **James W. Edwards**, Austin; **William R. Pitts**, Round Rock; **Michael S. Butler**, Austin, all of Tex.

[73] Assignee: **National Instruments Corporation**, Austin, Tex.

[21] Appl. No.: **08/979,968**

[22] Filed: **Nov. 26, 1997**

[51] **Int. Cl.**[6] **G06F 13/00**

[52] **U.S. Cl.** **710/129**; 714/27

[58] **Field of Search** 395/183.03, 183.21, 395/200.54, 280, 306, 309; 439/255; 714/27, 45; 710/100, 126, 129; 709/224

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,829,244	5/1989	Tom et al.	324/158 F
5,775,955	7/1998	Graube et al.	439/717

OTHER PUBLICATIONS

Product information "PCMCIA Interface Card" DeviceNet, 1998, Open DeviceNet Vendor Association, Inc., pp. 23, 1 sheet.

Product information PCMCIA interface Card: 5136-DN-PCM Direct-Link adapter for DeviceNet, 1991, 1 sheet.

Product Preview "Interface card provides ISADeviceNet link," Control Engineering, Jul. 1995, pp. 99, 1 sheet.

Instrumentation Reference and Catalogue 1997: Test Measurement and Industrial Automation, pp. 6-39 6-42.

Application Controller CAN-AC1/AC2 Data Sheet, originally printed from "Softing" website May 28, 1997 (2 sheets).

PCI Process Control Interface pp. 12, from "Softing" brochure dated Sep. 1995.

CAN-PCMICIA: PCMCIA Interface Product information from "CAN Solutions '97" at http://www/actia.com.

ICT data sheet for Foundation Fieldbus H1 interface, from "Softing" brochure dated Jan. 1995 (2 sheets).

Primary Examiner—Glenn A. Auve

Attorney, Agent, or Firm—Conley, Rose & Tayon; Jeffrey C. Hood; Georgious Georgakis

[57] **ABSTRACT**

An improved dual-connector cable for connecting a computer to a serial instrumentation bus. In one embodiment, the serial instrumentation bus is a fieldbus, preferably either a Foundation fieldbus or a Controller Area Network (CAN) bus. The cable comprises a first terminal located at a first end of the cable for coupling the cable to the computer. The first terminal comprises a device connector which is configured to connect the first terminal to a connector on the computer. The cable also comprises a second terminal located at a second end of the cable for coupling the cable to the serial instrumentation bus. The second terminal comprises interface circuitry for interfacing the cable with the serial instrumentation bus. The second terminal further comprises a first bus connector that is electrically coupled to the serial instrumentation interface circuitry. The first bus connector is configured to connect to a mating connector for coupling to the serial instrumentation bus. The second terminal further comprises a second bus connector that is electrically coupled to the serial instrumentation interface circuitry. The second bus connector is configured to connect to the serial instrumentation bus. In one embodiment, the first bus connector is operable to be connected to the serial instrumentation bus and the second bus connector is operable to be connected to a bus monitor to enable the bus monitor to monitor signals on the serial instrumentation bus.

22 Claims, 11 Drawing Sheets

US005596169A

United States Patent [19]

Baker et al.

[11] **Patent Number: 5,596,169**

[45] **Date of Patent: Jan. 21, 1997**

[54] **COMBINED SCSI/PARALLEL PORT CABLE**

[75] Inventors: **William P. Baker**, Salt Lake City; **Charles Hamilton**, Bountiful, both of Utah

[73] Assignee: **Iomega Corporation**, Roy, Utah

[21] Appl. No.: **439,776**

[22] Filed: **May 12, 1995**

[51] **Int. Cl.**[6] **H01B 11/02**

[52] **U.S. Cl.** **174/33**; 174/34; 341/89; 439/505

[58] **Field of Search** 174/33, 27, 32, 174/34; 361/686; 439/65; 341/89, 100, 101

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,603,320	7/1986	Farago	340/347 DD
4,864,291	9/1989	Korpi	340/825.5
4,941,845	7/1990	Eppley et al.	439/505 X
4,972,470	11/1990	Farago	380/3
5,031,115	7/1991	Hayashi	364/519
5,099,137	3/1992	Lattin, Jr.	307/147
5,101,481	3/1992	Anger et al.	395/325
5,119,498	6/1992	McNeill et al.	395/800
5,150,465	9/1992	Bush et al.	395/275
5,195,022	3/1993	Hoppal et al.	361/391 X
5,245,558	9/1993	Hachey	364/708.1 X
5,245,703	9/1993	Hubert	395/200
5,289,580	2/1994	Latif et al.	395/275
5,321,819	6/1994	Szczepanek	395/325
5,457,785	10/1995	Kikinis et al.	395/308 X

Primary Examiner—Kristine L. Kincaid
Assistant Examiner—Chau N. Nguyen
Attorney, Agent, or Firm—Woodcock, Washburn, Kurtz, Mackiewicz & Norris

[57] **ABSTRACT**

A cable for connecting a peripheral device to an input/output port configured in accordance with either a SCSI protocol or a parallel port protocol has a first connector which has a plurality of contact pins for connecting the cable to the peripheral device; a second connector which has a plurality of contact pins for connecting the cable to the input/output port; and a plurality of twisted pairs each having a first conductor and a second conductor. The first conductor of each of the twisted pairs is a data/control line, and the second conductor of the twisted pair is a return for the respective data/control line in accordance with the SCSI protocol. The first and second conductors of each of the twisted pairs are connected between selected pins of the first and second connectors such that none of the twisted pairs carries a data/control signal on both its first and second conductors when the cable is connected to an input/output port that is configured in accordance with the parallel port protocol.

6 Claims, 3 Drawing Sheets

(12) **United States Patent**
Reddersen et al.

(10) **Patent No.: US 6,293,467 B1**
(45) **Date of Patent: *Sep. 25, 2001**

(54) **MULTIPLE-INTERFACE SELECTION SYSTEM FOR COMPUTER PERIPHERALS**

(75) Inventors: **Brad R. Reddersen; Phillip W. Shepard; Rockie D. Moch; Jon Paul Charles Williams**, all of Eugene, OR (US)

(73) Assignee: **PSC Scanning, Inc.**, Eugene, OR (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/268,263**

(22) Filed: **Mar. 15, 1999**

Related U.S. Application Data

(62) Division of application No. 08/955,864, filed on Oct. 21, 1997, now Pat. No. 5,905,249, which is a continuation of application No. 08/706,736, filed on Sep. 9, 1996, now Pat. No. 5,703,347, which is a continuation of application No. 08/305,517, filed on Sep. 13, 1994, now Pat. No. 5,563,402.

(52) U.S. Cl. 235/462.15; 235/462.13

(58) Field of Search 235/467.13, 462.15, 235/462.07; 439/59, 65, 68, 502, 620

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,543,450	9/1985	Brandt	179/2
4,579,407 •	4/1986	Shimada	439/29 R

(List continued on next page.)

Primary Examiner—Karl D. Frech
(74) *Attorney, Agent, or Firm*—Lyon & Lyon LLP

(57) **ABSTRACT**

An interface selection and configuration system for a computer peripheral in which configuration for the peripheral and/or the host interface is at least in part accomplished by the interface connector cable. In a preferred embodiment, the computer peripheral is equipped with one or more hardware interfaces. The interface connector cable has a first end connector for attaching to the computer peripheral. The first end connector of the interface connector cable is typically a multiple pin connector constructed and arranged to be properly physically and electrically connectable only to a specific computer peripheral or class of computer peripherals, the first end connector including at least one electrical connection between two pins for completing a circuit within the computer peripheral thereby enabling the computer peripheral. Where the peripheral is a data reading device such as a laser scanner or RFID reader, alternate or

US006058604A

United States Patent [19]

Goodfellow

[11] **Patent Number: 6,058,604**

[45] **Date of Patent: May 9, 2000**

[54] **CABLE FOR ALLOWING MASS STORAGE DEVICE ADDRESS SELECTION**

[76] Inventor: **Tony Goodfellow**, 6662 Gatehill Cir., Huntington Beach, Calif. 92648

[21] Appl. No.: **08/971,227**

[22] Filed: **Nov. 15, 1997**

[51] **Int. Cl.**[7] **H01R 43/16**

[52] **U.S. Cl.** **29/874**; 29/747; 29/748; 29/749; 29/750; 29/865; 29/866; 29/884; 439/49; 439/119; 439/329; 439/346; 439/391; 439/426; 439/494

[58] **Field of Search** 29/749, 747, 865, 29/748, 866, 750, 867, 874, 884; 439/49, 50, 52, 53, 77, 95, 96, 98, 99, 119, 329, 346, 389, 391, 426, 494

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,850,899	7/1989	Maynard	439/628
5,326,286	7/1994	Bixler et al.	439/751 X
5,465,479	11/1995	Bowen et al.	29/749 X
5,601,444	2/1997	Cox	439/299 X
5,794,014	8/1998	Shetty et al.	395/500
5,805,921	9/1998	Kikinis et al.	395/822
5,905,885	5/1999	Richter et al.	395/500 X

OTHER PUBLICATIONS

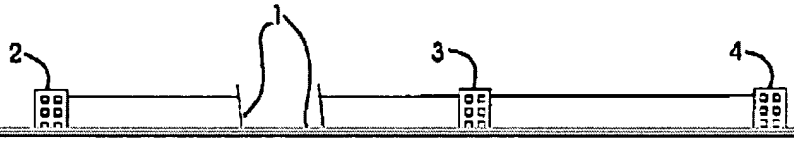
Application, pp. 1–5 Tony Goodfellow, Cable Construction Method to Allow Mass Storage Device Address Selection by Means of its Position on a Cable, Nov. 15, 1997.

Primary Examiner—Lee Young
Assistant Examiner—Binh-An Nguyen
Attorney, Agent, or Firm—Christie, Parker & Hale, LLP

[57] **ABSTRACT**

A cable constructed with insulation displacement connectors produces cables which connect data storage devices to a host system. The cable allows automatic address selection of data storage devices depending on the presence or absence of a CSEL terminal pin on a corresponding connector and the location of a data storage device along the cable. Address selection by connector configuration simplifies cable construction. The end connector of an ATA cable is configured to identify an attached data storage device as the first device (drive 0), while an intermediate connector is configured to identify an attached data storage device as the second drive (drive 1), thus making installation more intuitive.

7 Claims, 2 Drawing Sheets



US006006295A

United States Patent [19]

Jones et al.

[11] Patent Number: 6,006,295

[45] Date of Patent: Dec. 21, 1999

[54] **TRANSLATOR WITH SELECTABLE FIFO FOR UNIVERSAL HUB CABLES FOR CONNECTING A PC'S PCMCIA OR PARALLEL PORTS TO VARIOUS PERIPHERALS USING IDE/ATAPI, SCSI, OR GENERAL I/O**

[75] Inventors: **Larry Lawson Jones**, Palo Alto; **Sreenath Mambakkam**, San Jose, both of Calif.

[73] Assignee: **On Spec Electronic, Inc.**, Santa Clara, Calif.

[21] Appl. No.: **08/869,624**

[22] Filed: **Jun. 5, 1997**

[51] **Int. Cl.**[6] **G06F 13/14**; G06F 13/20

[52] **U.S. Cl.** **710/62**; 710/8; 710/11; 710/63; 709/230; 395/500.48; 395/527; 340/825.04

[58] **Field of Search** 395/500, 882, 395/883, 200.6, 831, 828, 500.48, 527; 340/825.04; 710/62, 63, 11, 8; 709/230

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,408,669	4/1995	Stewart et al.	395/750
5,430,847	7/1995	Bradley et al.	395/325
5,454,085	9/1995	Gajjar et al.	395/285
5,457,785	10/1995	Kikinis et al.	395/308
5,535,371	7/1996	Stewart et al.	395/500
5,540,597	7/1996	Budman et al.	439/77
5,540,601	7/1996	Botchek	439/502
5,570,002	10/1996	Castleman	323/285
5,576,698	11/1996	Card et al.	340/825.52
5,596,169	1/1997	Baker et al.	174/33
5,640,541	6/1997	Bartram et al.	395/500
5,729,204	3/1998	Fackler et al.	340/825.04
5,828,905	10/1998	Rao	395/883

Primary Examiner—Thomas C. Lee
Assistant Examiner—Rehana Perveen
Attorney, Agent, or Firm—Stuart T. Auvinen

[57] **ABSTRACT**

A universal cable connects a personal computer's parallel port or PCMCIA socket to a variety of types of external peripheral devices. The universal cable contains a translator circuit that converts signals from the parallel port or PCMCIA socket to external interface signals. The translator circuit combines together bytes from the parallel port to out put words when the external peripheral is an IDE or ATAPI device, or a subset of the ISA or AT bus. The translator circuit passes bytes through to 8-bit SCSI peripherals. The 16 data bits from the PCMCIA socket are passed through to IDE, ATAPI, and ISA devices, but split into bytes for SCSI devices. General-purpose I/O for external peripherals is also supported using separate input and output signals rather than bi-directional I/O. Software on the personal computer controls the configuration of the translator circuit, allowing the universal cable to be re-configured for different types of external peripherals. A 36-pin IEEE 1248-C connector is used to connect the universal cable to various external peripherals. A printer pass-through connector is provided on the translator's housing.

13 Claims, 10 Drawing Sheets

US005703347A

United States Patent [19]

Reddersen et al.

[11] Patent Number: 5,703,347

[45] Date of Patent: *Dec. 30, 1997

[54] MULTIPLE-INTERFACE SELECTION SYSTEM FOR COMPUTER PERIPHERALS

[75] Inventors: Brad R. Reddersen; Phillip W. Shepard; Rockie D. Moch; Jon Paul Charles Williams, all of Eugene, Oreg.

[73] Assignee: Spectra-Physics Scanning Systems, Inc., Eugene, Oreg.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,347,113.

[21] Appl. No.: 706,736

[22] Filed: Sep. 9, 1996

Related U.S. Application Data

[63] Continuation of Ser. No. 305,517, Sep. 13, 1994, Pat. No. 5,563,402, which is a continuation-in-part of Ser. No. 39,606, Mar. 25, 1993, Pat. No. 5,347,113, which is a continuation-in-part of Ser. No. 34,189, Mar. 22, 1993, Pat. No. 5,330,370, which is a continuation of Ser. No. 788,267, Nov. 4, 1991, abandoned.

[51] Int. Cl.[6] G06K 7/10

[52] U.S. Cl. 235/472; 235/462

[58] Field of Search 235/462, 472, 235/436; 439/329, 488, 489, 491, 620, 502

[56] References Cited

U.S. PATENT DOCUMENTS

4,579,407	4/1986	Shimada	439/620
4,678,288	7/1987	Lonsdale et al.	350/432
4,694,182	9/1987	Howard	250/566
4,699,447	10/1987	Howard	350/6.9
4,820,193	4/1989	Noonily	439/488
4,889,497	12/1989	Riches	439/620
4,902,244	2/1990	Endo et al.	439/488
4,915,639	4/1990	Cohn et al.	439/488
4,941,845	7/1990	Eppley et al.	439/505
4,954,101	9/1990	Nelson	439/502
5,040,993	8/1991	Krug et al.	439/620
5,092,793	3/1992	Stephan	235/472 X
5,181,858	1/1993	Matz et al.	439/489
5,214,268	5/1993	Doing	235/462
5,222,164	6/1993	Bass, Sr. et al.	438/488
5,250,792	10/1993	Swartz et al.	235/472
5,330,370	7/1994	Reddersen et al.	439/502
5,347,113	9/1994	Reddersen et al.	235/462
5,563,402	10/1996	Reddersen et al.	235/436

Primary Examiner—Donald T. Hajec
Assistant Examiner—Karl D. Frech
Attorney, Agent, or Firm—Lyon & Lyon LLP

[57] ABSTRACT

An interface selection and configuration system for a computer peripheral in which configuration for the peripheral and/or the host interface is at least in part accomplished by the interface connector cable. In a preferred embodiment, the computer peripheral is equipped with one or more hardware interfaces. The interface connector cable has a first end connector for attaching to the computer peripheral. The first end connector of the interface connector cable is typically a multiple pin connector constructed and arranged to be properly physically and electrically connectable only to a specific computer peripheral or class of computer peripherals, the first end connector including at least one electrical connection between two pins for completing a circuit within the computer peripheral thereby enabling the computer peripheral. Where the peripheral is a data reading device such as a laser scanner or RFID reader, alternate or additional configuration may be obtained, with data reading device, from the label on the interconnect cable. The label, which may for example be a bar code or RFID tag, contains information or instructions by which the data reading device

United States Patent [19]

Tomer

[11] **Patent Number: 4,836,799**

[45] **Date of Patent: Jun. 6, 1989**

[54] ELECTRICAL CABLE CONNECTOR

[76] Inventor: **Jitendra P. Tomer**, 169 Castlefrank Rd., Kanata, Ontario, Canada, K2L 1T3

[21] Appl. No.: **155,758**

[22] Filed: **Feb. 16, 1988**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 21,800, Mar. 4, 1987, abandoned.

[51] **Int. Cl.**[4] **H01R 13/28**

[52] **U.S. Cl.** **439/284**; 439/289; 439/507

[58] **Field of Search** 439/284, 286, 287, 289-291, 439/507, 510-512, 597, 722, 723

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,638,164	1/1972	Glance et al.	439/284
4,501,459	2/1985	Chandler et al.	439/289
4,666,231	5/1987	Sheesley et al.	439/507

Primary Examiner—P. Austin Bradley
Attorney, Agent, or Firm—Pascal & Associates

[57] **ABSTRACT**

An electrical cable connector configured to physically and electrically mate and connect with an indentical such electrical cable connector. The cable connector includes both male and female connectors corresponding to each circuit lead of the cable configured to mate and electrically connect with the female and male connectors, respectively, corresponding to like circuit leads of another identical cable connector. The male connector is electrically insulated from its associated circuit lead when the cable connector is not electrically connected to a second cable conector and is electrically connected to the circuit lead when the cable connector is electrically connected to a second cable connector. The male connector is preferably a pin and the female connector a socket comprising two terminals electrically insulated from one antoher. The male pin is electrically connected to one of the terminals of the female socket. The other terminal of the female socket is electrically connected to the circuit lead with which the male pin and female socket are associated. The circuit between the pin and the circuit lead is completed through the associated socket when the pin of an identical such cable connector makes contact with both terminals of the socket.

7 Claims, 3 Drawing Sheets

US006301633B1

(12) **United States Patent**
Chapman

(10) **Patent No.: US 6,301,633 B1**
(45) **Date of Patent: *Oct. 9, 2001**

(54) **GENERIC SERIAL INTERFACE WITH AUTOMATIC RECONFIGURABILITY**

(75) Inventor: **John T. Chapman**, Cupertino, CA (US)

(73) Assignee: **Cisco Technology, Inc.**, San Jose, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/520,411**

(22) Filed: **Mar. 8, 2000**

Related U.S. Application Data

(62) Division of application No. 09/001,352, filed on Dec. 31, 1997.

(51) **Int. Cl.**[7] **G06F 13/00**; G06F 13/38

(52) **U.S. Cl.** **710/129**; 710/126; 710/62; 710/63; 710/104; 439/189; 439/497; 326/30

(58) **Field of Search** 710/129, 100, 710/126, 128, 131, 62, 63, 8, 10, 11, 15, 16, 72, 73, 104; 439/189, 507, 497, 509; 326/30

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,607,379	*	8/1986	Marshall, Jr. et al.	375/377
4,887,260	*	12/1989	Carden et al.	370/250
5,648,972	*	7/1997	Gharakhanian	714/716
5,737,364	*	4/1998	Cohen et al.	375/220
5,761,463	*	6/1998	Allen	710/129

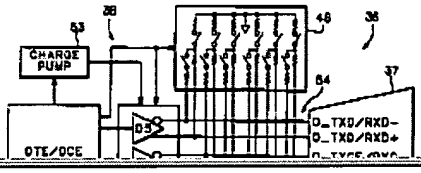
* cited by examiner

Primary Examiner—Rupal Dharia
(74) *Attorney, Agent, or Firm*—Marger Johnson & McCollom, P.C.

(57) **ABSTRACT**

A generic serial interface includes any one of multiple transition cables having a first connector conforming to one of several different serial interface standards. A second generic connector is connected to a second end of the transition cables. A configurable interface circuit is coupled to the generic connector and is automatically reconfigured according to the physical interface type associated with the transition cable. The interface circuit includes a termination resistor array that can connect different termination resistor values to the same generic signals on the generic connector according to the interface type. The termination resistor array in combination with a unique designation of generic signals allow a single interface to operate with many different serial interface standards both in DCE and DTE modes while requiring substantially fewer connector pins and simpler interface circuitry than existing generic interfaces.

13 Claims, 20 Drawing Sheets



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(module or device or unit) and connector and pin an Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **High-density and high-pin count flexible SMD connector for high-sp data bus**
Sasaki, S.; Kishimoto, T.;
Electronic Manufacturing Technology Symposium, 1993, Fifteenth IEEE/CHMT International , 4-6 Oct. 1993
Pages:411 - 416

[Abstract] [PDF Full-Text (588 KB)] **IEEE CNF**

---

2 **A common-mode current measurement technique for EMI performa evaluation of PCB structures**
Ye, X.N.; Hochanson, D.M.; Drewniak, J.L.;
Environmental Electromagnetics, 2000. CEEM 2000. Proceedings. Asia-Pacific Conference on , 3-7 May 2000
Pages:389 - 394

[Abstract] [PDF Full-Text (360 KB)] **IEEE CNF**

---

3 **An optical active connector: an optical interconnect module with an electrical connector interface**
Sasaki, S.; Tanaka, N.; Yamaguchi, S.; Nakamura, M.; Hayashi, T.;
Electronic Components and Technology Conference, 1996. Proceedings., 46th 31 May 1996
Pages:512 - 519

[Abstract] [PDF Full-Text (1316 KB)] **IEEE CNF**

---

4 **EMI associated with inter-board connection for module-on-backpla and stacked-card configurations**
Ye, X.; Nadolny, J.; Drewniak, J.L.; Hubing, T.H.; Vaudoren, T.P.; DuBroff, D.

Electromagnetic Compatibility, 1999 IEEE International Symposium on , Volu
2 , 2-6 Aug. 1999
Pages:797 - 802 vol.2

[Abstract] [PDF Full-Text (520 KB)] IEEE CNF

---

5 **Receiver Fixture Interface (RFI) IEEE P1505 system standard**
Stora, M.J.;
AUTOTESTCON '99. IEEE Systems Readiness Technology Conference, 1999.
IEEE , 30 Aug.-2 Sept. 1999
Pages:787 - 799

[Abstract] [PDF Full-Text (828 KB)] IEEE CNF

---

6 **A compact optical active connector: an optical interconnect module an electrical connector interface**
Sasaki, S.; Tanaka, N.; Ando, Y.; Yamaguchi, S.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 22 , Issue: 4 , Nov. 1999
Pages:541 - 550

[Abstract] [PDF Full-Text (1372 KB)] IEEE JNL

---

7 **High-speed signal transmission at the front of a bookshelf packagin system**
Koike, S.; Kaizu, K.; Kishimoto, T.;
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on] , Volume: 20 , Issue: 4 , N
1997
Pages:353 - 360

[Abstract] [PDF Full-Text (236 KB)] IEEE JNL

---

8 **High performance mainframe computer cables**
Beaman, B.;
Electronic Components and Technology Conference, 1997. Proceedings., 47th
21 May 1997
Pages:911 - 917

[Abstract] [PDF Full-Text (612 KB)] IEEE CNF

---

9 **A compact optical active connector: An optical interconnect module an electrical connector interface**
Sasaki, S.; Ando, Y.; Tanaka, N.; Yamaguchi, S.;
Electronic Components and Technology Conference, 1998. 48th IEEE , 25-28
1998
Pages:210 - 217

[Abstract] [PDF Full-Text (1416 KB)] IEEE CNF

---

10 **Signal conditioning electronics and packaging for the Alcator C-MO**

tokamak
Parkin, W.;
Fusion Engineering, 1991. Proceedings., 14th IEEE/NPSS Symposium on , 30 Sept.-3 Oct. 1991
Pages:790 - 793 vol.2

[Abstract] [PDF Full-Text (408 KB)] **IEEE CNF**

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L3: Entry 1 of 20 File: USPT Feb 24, 2004

DOCUMENT-IDENTIFIER: US 6697892 B1
TITLE: Port expansion system

Detailed Description Text (20):
FIG. 12 is a more detailed block diagram of a practical embodiment of a hub end module 300 that may be used as the "front end" of a port expansion system in accordance with the invention. The module 300, as well as the other modules of the system, utilizes standard, commercially available electrical and electronic components whose specifications and operation are well known in the art and therefore need not be described in detail. The principal component of the hub end module is a 7-port USB hub controller 302 which can support up to seven downstream USB slave ports denoted in FIG. 12 as "Port-1" through "Port-7". These ports are defined by sets of contacts on a downstream DB-25 connector receptacle or jack 304 carried by the module 300. The hub end module 300 further includes host USB port comprising a standard 4-pin USB Type-A connector 306 for connecting the module by means of a standard USB cable to a USB port on a host system such as a notebook computer. As already explained, the DB-25 jack 304 is connectable to a mating upstream DB-25 plug on any peripheral device module, or to a power end module.

Detailed Description Text (32):
FIG. 15 is a block diagram depicting the general form of a peripheral device module 360, and includes a DB-25 plug 362 on the upstream side of the module and a DB-25 jack or receptacle 364 on the downstream side. The pin assignments for the connectors 362 and 364 are as shown in FIG. 13. The module 360 includes pass-through power bus (VCCBUS), VCCSEL control signal, and ground lines 366, 368 and 370, respectively. The module 360 includes an interface circuit, for example, a controller 372 providing conversion of the USB data signals appearing on "Port-1" of the DB-25 plug 362 to the protocol of the peripheral device adapted to be connected to the device or function connectors 374 supported by the module. The typical module 360 includes an LED display 376 responsive to status and/or activity signals generated by the interface circuit 372.

L4: Entry 19 of 21 File: USPT Feb 19, 1985

DOCUMENT-IDENTIFIER: US 4500933 A
TITLE: Universal interface unit

Detailed Description Text (5):
When a recorder is connected to the synchronizer, input information relating to the recorder is provided as an address signal to the memory unit 14. Typically, a recorder is connected to a synchronizer by means of multi-pin connectors. Some of the pins of such a connector can be used to provide the input information regarding the personality of the particular recorder. In the embodiment of FIG. 1, three of the pins 16 on the synchronizer connector are connected to a positive potential V through appropriate bias resistors 18. Another pin 20 is directly connected to ground. By selectively connecting the pins 16 to the ground pin 20, a binary input signal relating to the control signal requirements of the recorder is provided to an address unit 22 connected to the pins 16. In the example illustrated in FIG. 1, a jumper 24 connected between the ground pin 20 and the middle pin 16 provides the binary signal 101 to the address unit 22. This binary signal identifies a particular recorder, or a group of recorders having the same input signal requirements. In response to this binary signal, the address unit 22 provides a suitable address signal to the memory unit 14. In turn, the memory unit 14 provides information to the processor 12 relating to the particular types of control signals that are to be applied to the recorder.

Current US Cross Reference Classification (3):
710/63

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L4: Entry 19 of 21 File: USPT Feb 19, 1985

US-PAT-NO: 4500933
DOCUMENT-IDENTIFIER: US 4500933 A

TITLE: Universal interface unit

DATE-ISSUED: February 19, 1985

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chan; Steven S.	Fremont	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Ampex Corporation	Redwood City	CA			02

APPL-NO: 06/ 364922 [PALM]
DATE FILED: April 2, 1982

INT-CL: [03] H03K 13/24, G11B 31/00

US-CL-ISSUED: 360/69; 364/200, 364/900
US-CL-CURRENT: 360/69; 360/48, 710/16, 710/63

FIELD-OF-SEARCH: 360/69, 364/200, 364/900

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4207687	June 1980	Haas et al.	35/12R

ART-UNIT: 235

PRIMARY-EXAMINER: Stellar; George G.

ATTY-AGENT-FIRM: LaBarre; James A. Talcott; Joel D.

ABSTRACT:

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A universal interface unit for providing output signals in any one of a plurality of different signal formats stores information relating to each of the different available formats. When signals are to be provided to a particular device, personality data regarding the device enables the particular signal format requirements of the device to be read from the stored information. A signal processor responsive to this information generates output signals in that format. The output signals are transmitted to the device through a switching circuit that is appropriately connected to the device to provide the proper polarity.

13 Claims, 4 Drawing figures

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L3: Entry 1 of 20 File: USPT Feb 24, 2004

US-PAT-NO: 6697892
DOCUMENT-IDENTIFIER: US 6697892 B1

TITLE: Port expansion system

DATE-ISSUED: February 24, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Laity; Ian A.	Simi Valley	CA		
Thornton; Timothy J.	Camarillo	CA		
Gu; George Q.	Northridge	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 569855 [PALM]
DATE FILED: May 12, 2000

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATION This application claims the benefit of provisional patent application Ser. No. 60/142,733 filed Jul. 8, 1999.

INT-CL: [07] G06 F 1/00

US-CL-ISSUED: 710/72; 710/63, 710/64, 710/314, 710/315, 710/317
US-CL-CURRENT: 710/72; 710/314, 710/315, 710/317, 710/63, 710/64

FIELD-OF-SEARCH: 710/301-304, 710/305-306, 710/311, 710/313, 710/314-317, 710/62-64, 710/65, 710/70, 710/71, 710/72, 710/73, 361/686

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4862353	August 1989	Williams	
☐	5220522	June 1993	Wilson et al.	710/304
☐	5460547	October 1995	Belt et al.	439/638
☐	5568356	October 1996	Schwartz	

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☐	5666495	September 1997	Yeh	710/301
☐	5699226	December 1997	Cavello	361/686
☐	5737189	April 1998	Kammersgard et al.	
☐	5805833	September 1998	Verdun	395/281
☐	5826042	October 1998	Kirkendoll	395/281
☐	5841424	November 1998	Kikinis	345/168
☐	5974492	October 1999	Gulick	710/107
☐	6049896	April 2000	Frank et al.	714/46
☐	6058441	May 2000	Shu	710/100
☐	6105143	August 2000	Kim	713/324
☐	6128743	October 2000	Rothenbaum	713/300
☐	6141719	October 2000	Rafferty et al.	710/131
☐	6243780	June 2001	Jun	710/305
☐	6286060	September 2001	DiGiorgio et al.	710/31
☐	6295519	September 2001	Wagner et al.	703/25
☐	6321340	November 2001	Shin et al.	713/310
☐	6424524	July 2002	Bovio et al.	361/686
☐	6493783	December 2002	Kinoshita et al.	710/303

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
3612034	October 1987	DE	
09059839	February 1997	JP	
WO9825352	June 1998	WO	

OTHER PUBLICATIONS

PCT International Search Report dated Feb. 11, 2000 re International application no. PCT/US 00/18707, international filing date Jul. 7, 2000.

ART-UNIT: 2181

PRIMARY-EXAMINER: Myers; Paul R.

ASSISTANT-EXAMINER: Phan; Raymond N

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman LLP

ABSTRACT:

A user configurable, modular port expansion system allows the user of a host system such as a USB-enabled personal computer to customize a desired configuration of one or more peripheral device modules without the use of cables between modules. The peripheral device modules are physically and electrically connectable to each other

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side-by-side between a hub end module and a power end module in any sequence so that there can be provided, within the limits of the host port specification, virtually any number of selected, expanded functions in any combination. The peripheral device modules may include, by way of example, a standard parallel DB-25 port module, a two-port serial PS/2 module, a two-port serial DB-9 module, a four- or seven-port USB hub, an RJ-11 Ethernet LAN module, and an RJ-11 modem module. Where the host port is USB compliant, power to the peripheral device modules may be supplied by the host system via a USB standard cable connected to the USB port of the hub end module, or, if more power is required, by an external a.c. power adapter connectable to the power end module. The power end module may also include an USB expansion port.

24 Claims, 22 Drawing figures

L3: Entry 2 of 20 File: USPT Jun 10, 2003

DOCUMENT-IDENTIFIER: US 6577507 B2
TITLE: Automatic circuit board plug-in system

Detailed Description Text (16):
A specific operation of the illustrative embodiment will be described with reference to FIGS. 5, 6 and 7. Assume that the plug-in control board 14 is in an active state. First, the operator inserts the circuit board 12 into the guide rails 20 and 22 and connects the control cable connectors 60 and 62 to the control cable connectors 28 and 30, respectively. As a result, the plug-in mechanisms 52 and 54 are electrically connected to the plug-in control board 14, so that the plug-in control unit 70 is ready to control the plug-in mechanisms 52 and 54. The operator then depresses the initialize switch 76 of the plug-in control board 14. In response, the initialize switch 76 sends out an initialization command 300 to the plug-in control unit 70.

Detailed Description Text (42):
As shown in FIG. 10, the signal sense pins 526 and 528 and power supply sense pins 530 and 532 of the mother board connector 16 are connected to the plug-in control unit 70 via the mother board connector 18 and a circuit board connector 82, which is mounted on the plug-in control board 14. In this arrangement, the loop circuit 525 assigned to signal pins includes the contacts 506 and 508 and pins 526 and 528 while the loop circuit 523 assigned to a power supply pin includes the contacts 510 and 512 and pins 530 and 532. The loop circuits 523 and 525 are connected to the plug-in control unit 70. The control unit 70 includes a loop detector circuit, not shown, adapted for determining whether the loop circuits 523 and 525 are open or closed. More specifically, the loop detector circuit is responsive to the conduction state between the signal pins 522 and 524 and the signal contacts 502 and 504 and the conduction state between the power supply pin 520 and the power supply contact 500.

Detailed Description Text (46):
Subsequently, the plug-in control unit 70 determines whether or not the input end of the loop circuit 525 responsive to the signal pins is in conduction, i.e., closed (step S90) If the input end is in conduction (Yes, step S90), then the control unit 70 executes a step S94. If the input end is not in conduction, i.e., open (No, step S90) , then the control unit 70 returns to the step S88 and again causes the stepping motors 204 to rotate forward by one step in synchronism with each other. As the control unit 70 repeats the steps S88 through S92, the circuit board connector 50 of the circuit board 12 is inserted deeper into the mother board connector 16 of the mother board 10. At the time when conduction is set up at the inlet end of the loop circuit 525, the signal sense contacts 506 and 508 of the circuit board connector 50 make contact with the signal sense pins 526 and 528 of the mother board connector 16, respectively. Consequently, a distance d shown in FIG. 11B becomes zero.

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L3: Entry 2 of 20 File: USPT Jun 10, 2003

US-PAT-NO: 6577507
DOCUMENT-IDENTIFIER: US 6577507 B2

TITLE: Automatic circuit board plug-in system

DATE-ISSUED: June 10, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kentaro	Tokyo			JP
Suzuki; Hiroshi	Chiba			JP
Kabe; Makoto	Chiba			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Oki Electric Industry Co., Ltd.	Tokyo			JP	03

APPL-NO: 10/ 231081 [PALM]
DATE FILED: August 30, 2002

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	2001-317737	October 16, 2001

INT-CL: [07] H05 K 5/00

US-CL-ISSUED: 361/754; 361/756, 361/759, 439/159
US-CL-CURRENT: 361/754; 361/756, 361/759, 439/159

FIELD-OF-SEARCH: 361/737, 361/724-727, 361/740, 361/741, 361/747, 361/754, 361/756, 361/759, 361/788, 361/798, 361/796, 361/801, 361/802, 439/159, 439/310, 439/177

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5619660	April 1997	Scheer et al.	395/282
☐	6345996	February 2002	Saito et al.	439/159
☐	6399887	April 2002	Lin	174/138D

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☐	6394828	May 2002	Kodama et al.	439/159
☐	6406322	June 2002	Barringer et al.	439/377

ART-UNIT: 2841

PRIMARY-EXAMINER: Martin; David

ASSISTANT-EXAMINER: Vu; Phuong T.

ATTY-AGENT-FIRM: Rabin & Berdo, P.C.

ABSTRACT:

A circuit board plug-in system includes a frame, a mother board mounted on the frame and including a mother board connector, and a circuit board including a circuit board connector capable of mating with the mother board connector. Guide rails are mounted on the frame, and each is formed with a channel for the insertion of the circuit board. An actuator moves, under the control of a plug-in controller, the circuit board inserted into the guide rails to thereby selectively connect or disconnect the circuit board connector to or from the mother board connector. The actuator is arranged partly on the circuit board and partly on the guide rails. The plug-in controller is mounted on the frame.

14 Claims, 19 Drawing figures

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L3: Entry 5 of 20 File: USPT Oct 16, 2001

DOCUMENT-IDENTIFIER: US 6304376 B1
TITLE: Fully automated telescope system with distributed intelligence

Detailed Description Text (14):
Each of the respective CLK and DATA signals of each of the respective 4-RJ11 connectors are electrically connected to a corresponding CLK and DATA signal pin of the 8-pin RJ11 connector 44. Thus, the AZ CLK and AZ DATA signal pins of connector 42 are coupled to pin 6 and 7, respectively of the 8-pin RJ11 connector. ALT CLK and ALT DATA are connected to pins 4 and 5, respectively, of connector 44 and AUX CLK and AUX DATA are connected, respectively, to pins 2 and 3 of connector 44. The source of each of these signals suitably comprises the hand-held control unit 36 which provides such signals over a flexible 8 conductor cable terminating in a male 8-pin RJ11 connector suitable for mating with the 8-pin connector 44 disposed on the electrical interface junction panel 30.

Detailed Description Text (51):
The internal construction of the semi-intelligent drive motor motion control unit 70 is illustrated in the schematic diagram of FIG. 5b. As can be seen, the operational focus of the motion control unit 70 is an EPROM/ROM based 8-bit microcontroller 88 exemplified by the PIC16C54, manufactured and sold by Microchip Technology, Inc. The function keys generally indicated at 89 described above in connection with FIG. 5a, provide inputs to the microcontroller 88 which, in response, develops control output signals which are directed to an 8-pin output header 90 having a pin configuration which corresponds to the 8-pin RJ11 connector (44 of FIG. 3b) of the electrical interface junction panel, to which the motion control unit 70 is intended to be connected. In response to the various direction, speed, focus and mode commands input to the microcontroller 88, the microcontroller develops and outputs control signals for the altitude motor (ALT CLK and ALT DATA), the azimuth motor (AZ CLK and AZ DATA), and a control signal pair for the auxiliary bus (AUX CLK and AUX DATA). Movement, speed, focus and mode commands are received by the microcontroller 88 and appropriate output control signals are developed thereby in accordance with a software or firmware program hosted by the microcontroller 88 and conventionally stored in an internal memory space such as a programmable ROM memory.

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L3: Entry 5 of 20 File: USPT Oct 16, 2001

US-PAT-NO: 6304376
DOCUMENT-IDENTIFIER: US 6304376 B1

TITLE: Fully automated telescope system with distributed intelligence

DATE-ISSUED: October 16, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Baun; Kenneth W.	Trabuco Canyon	CA		
Smith; John E.	Mission Viejo	CA		
Hoot; John E.	San Clemente	CA		
Wachala; Michael A.	Riverside	CA		
Tingey; Brian G.	Fountain Valley	CA		
Duchon; Brent G.	Garden Grove	CA		
Dewan; Stanley H.	Rancho Santa Margarita	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Meade Instruments Corporation	Irvine	CA			02

APPL-NO: 09/ 551332 [PALM]
DATE FILED: April 18, 2000

PARENT-CASE:
PRIORITY CLAIM This application is a division of patent application Ser. No.09/428,865, filed Oct. 26, 1999, entitled "FULLY AUTOMATED TELESCOPE SYSTEM WITH DISTRIBUTED INTELLIGENCE" which takes priority from provisional patent application Ser. No. 60/105,626, filed Oct. 26, 1998 entitled "FULLY AUTOMATED TELESCOPE SYSTEM WITH DISTRIBUTED INTELLIGENCE" and provisional patent application Ser. No. 60/143,637, filed Jul. 14, 1999, entitled "SELF ORIENTING, SELF ALIGNING, INTUITIVE AUTOMATED TELESCOPE", the entire contents of which are expressly incorporated herein by reference.

INT-CL: [07] G02 B 23/00, H02 P 1/00, G05 G 5/00, G05 B 5/00

US-CL-ISSUED: 359/429; 318/626, 318/266, 318/467
US-CL-CURRENT: 359/429; 318/266, 318/467, 318/626

FIELD-OF-SEARCH: 359/429, 359/430, 250/201, 250/203.1, 318/626, 318/652, 318/286, 318/466, 318/467, 318/468, 318/469, 318/470, 318/266, 318/600, 318/625

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4682091	July 1987	Krewalk et al.	318/685
☐	4764881	August 1988	Gagnon	364/559
☐	5555160	September 1996	Tawara et al.	362/31
☐	5822116	October 1998	Leblanc	359/430
☐	5828814	October 1998	Cyman et al.	395/102
☐	5912541	June 1999	Bigler et al.	318/625
☐	6108277	August 2000	Whitmore	368/18

ART-UNIT: 282

PRIMARY-EXAMINER: Spyrou; Cassandra

ASSISTANT-EXAMINER: Winstedt; Jennifer

ATTY-AGENT-FIRM: Stradling Yocca Carlson & Rauth

ABSTRACT:

A fully automated telescope system is able to be fully operable in both Alt-Az and polar configurations. In either configuration, the telescope aligns itself to be celestial coordinate system following a simplified initialization procedure during which the telescope tube is first pointed north and then pointed towards a user's horizon. A command processor, under application software program control orients the telescope system with respect to the celestial coordinate system given the initial directional inputs. The initial telescope orientation may be further refined by initially inputting a geographical location indicia, or by shooting one or two additional celestial objects. Once the telescope's orientation with respect to the celestial coordinate system is established, the telescope system will automatically move to and track any desired celestial object without further alignment invention by a user.

31 Claims, 27 Drawing figures

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L3: Entry 6 of 20 File: USPT Sep 25, 2001

DOCUMENT-IDENTIFIER: US 6295481 B1
TITLE: Serial bus control system for sewing equipment

Brief Summary Text (14):
A series of modules are mounted along the length of the serial bus cable and are connected to the serial bus cable with snap or press-fit type connectors to enable easy installation and removal of the modules from the serial bus cable for ease of replacement. The modules include a memory module that stores system data for error monitoring, production information, and adjustable values that affect machine operation. A program module stores a copy of the operation program for the automatic sewing equipment. The serial bus control system further includes at least one input module that is connected to the sensors for the sewing equipment. The input module receives and transmits information regarding the position and movement of the work pieces as detected by the sensors to the system controller. One or more output modules are also connected to the serial bus cable, with each output module being linked to different assembly or series of devices of the automated sewing equipment, such as the sewing machine with its sewing needle and knife, the drive rollers, as well as the movement of the folder tongue of the folder assembly.

Brief Summary Text (15):
Each module generally is preprogrammed with a generic function or series of functions based upon the type of module. Each module further is programmed with an identifier such as a serial number that serves to uniquely identify that module. During the initial set-up of the serial bus control system of the present invention, after the memory module and program module have been installed, each of the input and output modules is individually installed one-by-one, as by fitting their mating connector into a corresponding connector positioned along the serial bus cable. As each module is added, the system controller scans the serial bus cable and records the pre-programmed serial number so as to identify the newly added module and assigns the proper routine or portion of the control software in the controller to control that module. The serial number and software assignment of each module are stored in the memory module of the serial bus control system and the modules and the system controller communicate with one another on the basis of these stored module serial numbers.

Drawing Description Text (7):
FIG. 5 is a perspective view schematically illustrating the serial bus cable with a connector and a module.

Detailed Description Text (19):
As illustrated 4C, the serial bus cable 125 connects at one of its ends to a power supply 132. The power supply generally is a 24 volt direct current switch mode power supply with built in surge suppression and power factor correction so as to accept power fluctuations in alternating current within a range of approximately 60 volts up to approximately 265 volts. The power supply places 24 volts of direct current on the serial bus, which is in turn supplied to the various operative assemblies of the sewing station by the serial bus cable as indicated in FIGS. 4A-4C. A series of 3 outlet connectors 133 connect the power supply to the serial bus cable and allow branching of one to three serial bus cables off the power supply. Each connector 133 is generally a 6-pin header connector manufactured by ITW

Panduit. As shown in FIGS. 1 and 4A, the serial bus control system 15 also includes a system controller 135 that typically is mounted above the work surface 24 (FIG. 1) of the work table 23 for access by the operator. The system controller 135 (FIG. 4A) typically comprises a computer or processing unit with a touch screen liquid crystal display 136 (FIG. 1). It also will be possible to use other types of input devices in place of the touch screen of the system controller such as a keyboard or keypad together with a monitor or display. The system controller can be a stand alone computer unit for the particular sewing station or can be linked to a computer network server or other computer systems at remote locations via a modem for remote monitoring and diagnostics. The operator inputs system commands and can monitor the performance of the sewing station in terms of down time due to fault conditions and other production information through the system controller.

Detailed Description Text (20):
As shown in FIGS. 4A-4C, a series of plug-in modules connect to the serial bus cable 125 at the connectors 128. The modules each generally include a circuit board 137 (FIG. 5), typically encased within a housing or plastic shrink warp 138, and having a series of electronic components including a processor chip 139, transceiver 141 for interfacing with the serial bus and a four-pin bus connector header 142 for connecting the module to a connector 128 of the serial bus cable as illustrated in FIG. 5. Each processor chip generally is an 8-bit microprocessor such as manufactured by MICROCHIP TECHNOLOGY, INC., and each generally is preprogrammed with a desired set of instructions or functions. As shown in FIG. 5, a series of contact pads or traces 143 generally formed from cooper, gold or similar electrically conductive material, are applied to the circuit board 137. These pads generally are contacts with connector pins of a programming device (not shown) for programming the processor chip of the module with desired instructions, which is typically a one-time programming operation.

Detailed Description Text (21):
Also, as illustrated in FIG. 5, each of the four-pin connector headers 142 that connect the modules to a connector of the serial bus cable typically include an L-shaped lead or pin 144 that is generally formed from a metal such as a copper alloy that is tin plated or similar electrically conductive material each having one end 146 soldered to the circuit board 137 and an opposite or free end 147 adapted to engage a connector 128 of the serial bus cable to form an electrical connection therewith. Each connector further includes a series of locking supports 148 through which the pins 144 are extended Each locking support generally is formed from a plastic material such as polyester and is substantially L-shaped, having a first end 149 that is mounted to the circuit board and a second end 151 that extends substantially parallel to the upper surface of the circuit board and which includes a locking tab or protrusion 152 that engages a retainer 129 of a connector 128 in a mating, locking relationship to lock the module to the connector and thus to the serial bus cable. The locking tabs 152 and flexible locking supports 148 enable the modules to be releasibly attached to the connectors of the serial bus cable in a snap or press fit type arrangement for ease of removable and replacement.

Detailed Description Text (22):
In addition, splices (not shown) having a similar construction to the four-pin bus connector headers of the modules can be received or locked into an unused connector of the serial bus cable. A female connector of an additional serial bus cable can then be attached to the connector of the first serial bus cable with the splice to enable additional serial bus cables to be connected in series or branched to the first serial bus cable as needed for controlling further operations for expanding the operation of the sewing station.

Detailed Description Text (23):
The modules include a series of different types of modules that perform different functions, including an adapter module 155, schematically illustrated in FIG. 6. The adapter module 155 includes a first, four-pin bus connector header 142 that

mates with and connects to the serial bus cable at one of its connectors 128. A second, five pin connector header 157 is provided at the opposite end of the adapter module and connects to the computer of the system controller to thus connect the system controller 135 (FIG. 4A). The adapter module includes a series of four transmission lines or connections 158A-158D between the two connectors 156 and 157, including two for the transmission of data 158C-158D, at least one power transmission line 158B and a ground 158A. The adapter module filters the power from the serial bus cable to the system controller and provides additional over-current or surge protection. Thus, power and data are passed directly through the adapter module from the serial bus cable into the system controller for powering the system controller and for transmitting and receiving data information and operation commands.

Detailed Description Text (24):
As shown in FIG. 4C, a program module 160 is mounted along the serial bus cable, typically at one end thereof, communicating with the system controller via the serial bus cable. As illustrated in FIG. 7, the program module 160 includes a four pin connector bus header 142 for attaching to a connector 128 (FIG. 5) for the serial bus cable 125 in a snap or press fit type arrangement to releasibly connect the program module to the serial bus cable. The program module includes a processor chip 139, and flash memory, indicated at 161, for storing program information. The program module stores a copy of the operating or control software for the serial bus control system that is executed in the system controller, thus functioning as RAM memory for the system controller.

Detailed Description Text (26):
A memory module 165 (FIGS. 4C and 8) is mounted on the serial bus cable 125 at a desired location, such as adjacent the program module. The memory module 155 includes a four pin bus connector header 142 (FIG. 8) for attachment of the memory module to the serial bus cable. The memory module 165 (FIG. 8) further includes an 8 bit processor chip 139, flash memory 166, and a clock or timer 167 for monitoring and recording data on a real time basis and providing the clock for the system controller. The memory module provides additional memory outside of the computer of the system controller for storing production data for the sewing station and real time stamped error logging and adjustable values affecting machine operation such as stitch counts, and operation/machine speeds.

Detailed Description Text (27):
As illustrated in FIGS. 4A-4B, a series of quad input modules 170 and opto-iso input modules 171 are mounted along the serial bus cable and connect to various input devices for the dewing station, such as thread breakage detectors, the upper edge guide, hem detect eye, raw edge guide and folded edge guide, as well as the tension sensor that provide input information as to the operation of the sewing station and which monitor and report the position and movement of the garment body therethrough. Generally, the serial bus control system will include one or more input modules depending upon the number of inputs for the sewing station. The quad input modules 170 (FIG. 9A) and opto-iso input modules 171 (FIG. 9B) both include a four pin bus connector header 142, by which the input modules are connected to a connector of the serial bus cable in the same fashion as the snap fit connections of the adapter, control and memory modules to the serial bus cable. Each input module further includes a processor 139 (FIGS. 9A and 9B), which is generally an 8 bit processor chip that is preprogrammed with a series of functions for processing input information regarding the movement, position and tensioning of the garment body as it is moved along the sewing path and for monitoring the operation of the sewing machine in response to signals from the various detectors and the foot pedals.

Detailed Description Text (29):
As shown in FIGS. 4B and 4C, the serial bus control system 15 further generally includes a series of quad output modules 180 and opto-iso output modules 181, each

of which includes a four-pin bus connector header 142 (FIGS. 10A and 10B) that attaches the modules to the serial bus cable in a snap or press type fitting to provide a quick release connection for each of the quad output modules and opto-iso output modules to the serial bus cable. As FIGS. 10A and 10B illustrate, each quad output and opto-iso output module includes a processor chip 139 that generally is preprogrammed with general instructions for performing a desired set of functions, such as controlling the motors for the upper and lower edge guides and for the upstream and downstream roller assemblies as illustrated in FIG. 4C.

Detailed Description Text (30):
Each quad output module, as shown in FIG. 10A, also includes a driver chip 182 for driving output instructions from the modules to the external devices such as solenoids 183 (FIG. 4C) for actuating an air valve for the upper edge guide and for controlling the operation of the folder tongue and stacker bar. A second connector header 184 (FIG. 10A), that generally is an eight-pin connector header which provides four independent current-sinking output channels for controlling a series of up to four different control devices, is mounted to the circuit board opposite the four-pin bus connector header 139. For example, as illustrated in FIG. 4C, a single output module is used for controlling the thread wipe 186, uncurler airjets 187, folder airjets 88 and folder tongue 43 in response to command signals received from the system controller via the serial bus cable. Similarly, as shown in FIG. 10B, each opto-iso output module 181 includes a second connector header 188 that typically is an eight-pin connector similar to the second connector header 184 (FIG. 10A) of each output module 180, but which optically isolates the output channels from each other and from the serial bus as illustrated in FIG. 10B. Typically the opto-iso output modules are used for control of devices such as the sewing machine of the sewing station.

CLAIMS:

1. A control system for automated sewing equipment of type having a sewing machine positioned along a sewing path along which a work piece is manipulated and sewn, and having a sewing needle, at least one detector for monitoring the work piece, and a drive system for moving the work piece about the sewing path, said control system comprising:

a system controller;

a serial bus system in communication with said system controller; and including:

a bus cable having a series of connectors therealong;

a program module having programmed instructions for operation of the sewing system;

at least one input module connected to said bus cable and to said at least one detector for communicating information from said detector to said system controller; and

at least one output module connected to said bus cable and to said sewing machine and drive system for communicating control instructions from said control module to said sewing machine and said drive system;

wherein each of said modules includes a connector adapted to releasibly engage a connector of said bus cable to enable ease of replacement of said modules.

11. A control system for a sewing station for sewing a work piece as the work piece is moved along a sewing path, the control system comprising:

a system controller for interfacing with an operator;

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a serial bus cable having a series of connectors attached therealong;

at least one input module connected to said bus cable for receiving and transmitting information about the operation of the sewing station to said system controller; and

at least one output module connected to said bus cable and receiving instructions from said system controller for controlling the operation of selected elements of the sewing station;

wherein said input and output modules each include a connector for enabling quick connection and disconnection of said modules from said bus cable for ease of set up and replacement of said modules.

23. The method of claim 21 and wherein the step of connecting input and output modules comprises fitting each module into a connector mounted along the serial bus cable.

26. The automated sewing station of claim 25 and wherein each of said input and output modules further comprises a connector adapted to releasably engage a connector positioned along said serial bus cable to enable quick connection and disconnection of said modules for easy replacement of said modules.

30. The method of claim 28 and wherein the step of connecting input and output modules comprises fitting each module into a connector mounted along the serial bus cable.

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L3: Entry 6 of 20 File: USPT Sep 25, 2001

US-PAT-NO: 6295481
DOCUMENT-IDENTIFIER: US 6295481 B1

TITLE: Serial bus control system for sewing equipment

DATE-ISSUED: September 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Price; George Alan	Lawrenceville	GA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
ECP Family Properties	Lawrenceville	GA			02

APPL-NO: 09/.275499 [PALM]
DATE FILED: March 24, 1999

INT-CL: [07] G06 G 19/00, D05 B 19/12

US-CL-ISSUED: 700/136; 112/470.05, 112/470.07
US-CL-CURRENT: 700/136; 112/470.05, 112/470.07

FIELD-OF-SEARCH: 700/136, 700/137, 700/138, 700/130, 112/470.05, 112/470.04, 112/470.01, 112/277, 112/470.07, 112/306, 112/153, 112/220, 112/475.03

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3818849	June 1974	Maddox, Jr.	112/275
☐	4481507	November 1984	Takiguchi et al.	340/679
☐	4867080	September 1989	Taylor et al.	112/80.32
☐	4924790	May 1990	Kondo et al.	112/272
☐	5042409	August 1991	Tanaka	112/306
☐	5161476	November 1992	Suzuki	112/306
☐	5269257	December 1993	Yamazaki	112/262
☐	5271347	December 1993	Carreras Fontcuberta	112/262

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☐	5437238	August 1995	Price et al.	112/470
☐	5498172	March 1996	Noda	439/404
☐	5509029	April 1996	Furuta	375/228
☐	5522332	June 1996	Price et al.	112/470
☐	5562060	October 1996	Price et al.	112/470
☐	5657711	August 1997	Price et al.	112/470
☐	5664962	September 1997	Noda	439/394
☐	5718183	February 1998	Shimizu et al.	112/275

OTHER PUBLICATIONS

Sunz Sensors S-LINK Sensor & Wire & Saving Link System of T Branch Multi Drop, Nov. 1994.

ART-UNIT: 375

PRIMARY-EXAMINER: Nerbun; Peter

ATTY-AGENT-FIRM: Womble Carlyle Sandridge & Rice PLLC

ABSTRACT:

A serial bus control system for an automatic sewing station for attaching a series of work pieces includes a serial bus cable connected to a power supply and a system controller. A program module is plugged into the serial bus cable and is programmed with an operations program or set of command instructions that are accessed and run by the system controller for controlling the automatic sewing station. A series of input modules are removably connected to the serial bus cable and receive inputs from various detectors monitoring the position and movement of the work pieces along a sewing path through the automatic sewing station. The input modules transmit this input information to the system controller via the serial bus cable in response to which the system controller sends command signals to a series of output modules that are connected to the operative elements of the sewing station, such as a sewing machine and upstream and downstream drive assemblies, to control the operation of the sewing machine and such other operative elements of the sewing station.

31 Claims, 14 Drawing figures

L3: Entry 9 of 20 File: USPT Feb 16, 1999

DOCUMENT-IDENTIFIER: US 5872999 A
TITLE: System for peripheral identification obtained by calculation and manipulation data collecting for determining communication mode and collecting data from first terminal contacts

Abstract Text (1):
A peripheral device for use with a data processing apparatus. The apparatus has a peripheral port with a set of terminal pins consisting of first to ninth pins disposed in a row. The first pin is assigned for one of a power source and the ground potential, the ninth pin for the other of the power source and the ground potential, the second, third, seventh and eighth pins for transmitting data signals, and the fourth to sixth for transmitting control signals. The apparatus has an element for selecting the communication mode of the peripheral device connected to the peripheral port, based on the data signals transmitted from the second, third, seventh and eighth pins. The peripheral device comprises a plug connector detachably connected to the peripheral port, the plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row, a cable including a plurality of wires connecting the terminal pins of the plug connector with terminals on an internal printed circuit board, and an element for transmitting data signals including identification data representing the communication mode via at least one of the second, third, seventh and eighth pins in synchronization with a clock signal supplied from the apparatus.

Brief Summary Text (19):
In order to achieve the objects, according to one aspect of the present invention, there is provided a peripheral device for use with a data processing apparatus, said apparatus having a peripheral port with a set of terminal pins consisting of first to ninth pins and being disposed in a row in the order of the first to the ninth pins, said first pin being assigned for connecting to one of a power source and the ground potential, said ninth pin being assigned for connecting to the other of the power source and the ground potential, said second, third, seventh and eighth pins being assigned for transmitting data signals, said fourth to sixth pins being assigned for transmitting control signals, said apparatus having means for selecting the communication mode for communicating with the peripheral device connected to the peripheral port based on the data signals transmitted from said second, third, seventh and eighth pins, said peripheral device comprising: a plug connector which is to be detachably connected to said peripheral port, said plug connector having a set of terminal pins consisting of first to ninth pins and being disposed in row in the order of the first to the ninth pins correspondingly to said first to ninth pins of the peripheral port; a cable including a plurality of wires connecting the terminal pins of said plug connector with terminals on a printed circuit board of said peripheral device; and means for transmitting data signals including identification data representing the communication mode of said peripheral device via at least one of said second, third, seventh and eighth pins in synchronization with a clock signal supplied from said apparatus when said plug connector is connected to said peripheral port.

Brief Summary Text (20):
According to another aspect of the invention, there is still provided a combination of a data processing apparatus and a peripheral device, comprising: said apparatus

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having a peripheral port with a plurality of terminal pins disposed in a row, said terminal pins including a pair of first pins, one assigned for connecting to one of a power source and the ground potential and the other assigned for connecting to the other of the power source and the ground potential, at least one of second pins assigned for transmitting data signals, a plurality of third pins assigned for transmitting control signals, said apparatus further having means for selecting the communication mode for communicating with the peripheral device connected to the peripheral port based on the data signals transmitted from said at least one second pin, means for transmitting a clock signal via one of said third pins to said peripheral device and means for performing a communication with the connected peripheral device with the selected communication mode; said peripheral device having a plug connector which is to be detachably connected to said peripheral port, said plug connector having a plurality of terminal pins configured as the same in number as and disposed in a row correspondingly to the terminal pins of said peripheral port, said peripheral device further having a cable including a plurality of wires connecting the terminal pins of said plug connector with terminal on a printed circuit board of said peripheral device and means for transmitting data signals including identification data representing the communication mode of said peripheral device via said at least one of second pin to said apparatus in synchronization with said clock signal when said plug connector is connected to said peripheral port.

Detailed Description Text (42):
Where the communication mode of a peripheral device is clocked parallel mode, the pin configuration of each plug 4ap (4bp) of the connectors are shown in FIG. 5B. In this mode, the apparatus 2 transmits to the controllers 3a and 3b a specified logical value ("1" or "0") as the peripheral selection signal TH and given clock signals as the data request signal TR. In response to this, signals of required logical values are then quickly provided through the data lines from the controllers 3a and 3b in synchronization with the clock signals. As shown in FIG. 5B, the pin 5 for the data request signal TR is short-circuited with the pin 6 for the peripheral acknowledgment signal TL in this clocked parallel communication mode, thereby the signals (voltages) on both the plug pins no. 5 and 6 being the same. Accordingly the signal TR transmitted from the apparatus 2 to pin no. 5 is sent back almost simultaneously from pin no. 6 to the apparatus 2 as the signal TL. Thus, the apparatus 2 identifies the clocked parallel mode by sensing signal TL equal to signal TR.

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L3: Entry 9 of 20 File: USPT Feb 16, 1999

US-PAT-NO: 5872999
DOCUMENT-IDENTIFIER: US 5872999 A

TITLE: System for peripheral identification obtained by calculation and manipulation data collecting for determining communication mode and collecting data from first terminal contacts

DATE-ISSUED: February 16, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Koizumi; Masahiro	Tokyo			JP
Niizuma; Naoki	Tokyo			JP
Kawase; Yasuhisa	Tokyo			JP
Ikebe; Hamjime	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sega Enterprises, Ltd.	Tokyo			JP	03

APPL-NO: 08/ 663215 [PALM]
DATE FILED: September 30, 1996

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This application is a Continuation-in-part of U.S. application Ser. No. 08/445,108 filed May 19, 1995 now U.S. Pat. No. 5,630,170.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	6/246580	October 12, 1994
JP	6/246581	October 12, 1994

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102(E)-DATE
PCT/JP95/02073	October 11, 1995	WO96/12250	Apr 25, 1996	Sep 30, 1996	Sep 30, 1996

INT-CL: [06] G06 F 13/36

US-CL-ISSUED: 395/892; 395/893, 463/1
US-CL-CURRENT: 710/72; 463/1

FIELD-OF-SEARCH: 395/828, 395/893, 364/410, 364/284, 364/240.1, 364/242.1, 463/1

PRIOR-ART-DISCLOSED:

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U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4501424	February 1985	Stone et al.	273/148B
☐	5059958	October 1991	Jacobs et al.	345/158
☐	5394168	February 1995	Smith, III et al.	345/156
☐	5630170	May 1997	Koizumi et al.	395/834

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
50-72547	June 1975	JP	
54-76034	June 1979	JP	
57-189231	November 1982	JP	
57-196333	December 1982	JP	
59-140559	August 1984	JP	
60-62299	April 1985	JP	
61-99233	June 1986	JP	
62-11955	January 1987	JP	
62-256066	November 1987	JP	
1-65654	March 1989	JP	
1-128153	May 1989	JP	
1-84155	June 1989	JP	
2-7147	January 1990	JP	
2-62618	March 1990	JP	
2-219160	August 1990	JP	
2-228718	September 1990	JP	
2-281364	November 1990	JP	
3-104971	October 1991	JP	
3-103571	October 1991	JP	
4-97472	March 1992	JP	
5-134973	June 1993	JP	

OTHER PUBLICATIONS

Copy of Office Action ("Notice of Reason for Rejection") of Japanese Patent Office for corresponding application No. Hei 8(1996)-511157 with full translation.

ART-UNIT: 272

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Chen; Anderson I.

ATTY-AGENT-FIRM: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

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ABSTRACT:

A peripheral device for use with a data processing apparatus. The apparatus has a peripheral port with a set of terminal pins consisting of first to ninth pins disposed in a row. The first pin is assigned for one of a power source and the ground potential, the ninth pin for the other of the power source and the ground potential, the second, third, seventh and eighth pins for transmitting data signals, and the fourth to sixth for transmitting control signals. The apparatus has an element for selecting the communication mode of the peripheral device connected to the peripheral port, based on the data signals transmitted from the second, third, seventh and eighth pins. The peripheral device comprises a plug connector detachably connected to the peripheral port, the plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row, a cable including a plurality of wires connecting the terminal pins of the plug connector with terminals on an internal printed circuit board, and an element for transmitting data signals including identification data representing the communication mode via at least one of the second, third, seventh and eighth pins in synchronization with a clock signal supplied from the apparatus.

24 Claims, 23 Drawing figures

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L3: Entry 13 of 20 File: USPT May 13, 1997

DOCUMENT-IDENTIFIER: US 5630170 A
TITLE: System and method for determining peripheral's communication mode over row of pins disposed in a socket connector

Abstract Text (1):
A peripheral device for use with a data processing apparatus. The apparatus has a peripheral port with a set of terminal pins consisting of first to ninth pins disposed in a row. The first pin is assigned for one of a power source and the ground potential, the ninth pin for the other of the power source and the ground potential, the second, third, seventh and eighth pins for transmitting data signals, and the fourth to sixth pins for transmitting control signals. The apparatus has an element for selecting the communication mode of the peripheral device connected to the peripheral port, based on the data signals transmitted from the second, third, seventh and eighth pins. The peripheral device comprises a plug connector detachably connected to the peripheral port, the plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row, a cable including a plurality of wires connecting the terminal pins of the plug connector with terminals on an internal printed circuit board, and an element for transmitting data signals including identification data representing the communication mode via at least one of the second, third, seventh and eighth pins in synchronization with a clock signal supplied from the apparatus.

Brief Summary Text (18):
According to one aspect of the invention, directed to one or more of the above objects, there is provided a peripheral device for use with a data processing apparatus having a peripheral port. The peripheral device includes a connector detachably connectable to the peripheral port, the connector having a set of terminal contacts including first to ninth contacts disposed in a row. The first contact is for connecting to one of a power source potential and ground potential; and the ninth contact is for connecting to the other of the power source potential and the ground potential. The second, third, seventh and eighth contacts are for transmitting data signals. The fourth to sixth contacts are for transmitting control signals. The apparatus further includes a cable including a plurality of wires connecting ones of the terminal contacts of the connector with a printed circuit board of the peripheral device and includes means for transmitting data signals including identification data representing a communication mode of the peripheral device to the data processing apparatus via at least one of the second, third, seventh and eighth contacts in synchronism with a clock signal supplied from the data processing apparatus when the connector is connected to the peripheral port.

Brief Summary Text (20):
Further, the peripheral device includes a plug connector detachably connectable to the peripheral port, the plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row correspondingly to the first to ninth pins of the peripheral port. The peripheral device further includes a cable including a plurality of wires connecting ones of the terminal pins of the plug connector with a printed circuit board of the peripheral device and means for transmitting data signals including identification data representing the communication mode of the peripheral device via at least one of the second, third, seventh and eighth pins in

synchronism with a clock signal supplied from the apparatus when the plug connector is connected to the peripheral port.

Brief Summary Text (22):
The game apparatus further includes a peripheral device having a plug connector detachably connected to the peripheral port, the plug connector having a plurality of contacts identical in number and disposed in a row in correspondence to the terminal pins of the peripheral port. The peripheral device further has a cable including a plurality of wires connecting the contacts of the plug connector with a printed circuit board of the peripheral device and means for transmitting data signals including identification data, representing the communication mode of the peripheral device via the at least one second pin to the data processing apparatus in synchronism with the clock signal when the plug connector is connected to peripheral port.

Detailed Description Text (42):
Where the communication mode of a peripheral device is clocked parallel mode, the pin configuration of each plug 4ap (4bp) of the connectors are shown in FIG. 5B. In this mode, the apparatus 2 transmits to the controllers 3a and 3b a specified logical value ("1" or "0") as the peripheral selection signal TH and given clock signals as the data request signal TR. In response to this, signals of required logical values are then quickly provided through the data lines from the controllers 3a and 3b in synchronization with the clock signals. As shown in FIG. 5B, the pin 5 for the data request signal TR is short-circuited with the pin 6 for the peripheral acknowledgment signal TL in this clocked parallel communication mode, thereby the signals (voltages) on both the plug pins no. 5 and 6 being the same. Accordingly the signal TR transmitted from the apparatus 2 to pin no. 5 is sent back almost simultaneously from pin no. 6 to the apparatus 2 as the signal TL. Thus, the apparatus 2 identifies the clocked parallel mode by sensing signal TL equal to signal TR.

Detailed Description Text (49):
FIG. 6A shows a controller 3a employing the TH/TR-selection type communication mode. "TH/TR selection type communication mode" used in this specification means a communication mode in which, as shown in Table 3, manipulation data which are generated in response to key switches on the peripheral device manipulated by an operator or a game player, as well as the identification data, are supplied to the data processing device in response to control signals. The control signals, as shown in Table 3 for example, are any of four combinations of two bit data TH and TR via the fourth and fifth pins. The controller 3a comprises the plug connector 4ap, the cable 5a having nine wires connected to the nine plug pin nos. 1 to 9 of the plug connector 4ap, and a main circuit 3M to which the wires of the cable 5a are connected. The nine plug pin nos. 1 to 9 are electrically independent from each other and individually connected to the nine wires of the cable 5a. The main circuit 3M has an operating portion 3Ma and a data generator 3Mb. The operating portion 3Ma, which is operated by a player, includes keys and/or switches. The data generator 3Mb is formed by circuits such as hardware logic circuits or a CPU system such that, as shown in Table 3, a specific group of 4-bit data R, L, D, U including data indicative of the TH/TR selection communication mode and data generated at the operating portion 3Ma by the player's operation are supplied through the plug pin nos. 2, 3, 7, 8 in response to, in Table 3, the 1st to 4th rows of bit patterns of both the peripheral selection signal TH and data request signal TR.

CLAIMS:

4. A peripheral device for use with a data processing apparatus, said apparatus having a peripheral port with a set of terminal pins consisting of first to ninth pins disposed in a row, said first pin for conducting one of power source and ground potential, said ninth pin for conducting the other of the power source and the ground potential, said second, third, seventh and eighth pins for conducting

data signals, said fourth and fifth pins for conducting control signals, said apparatus having means for determining a communication mode for communicating with a peripheral device connected to the peripheral port based on the data signals received on said second, third, seventh and eighth pins, said peripheral device comprising;

a plug connector detachably connectable to said peripheral port, said plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row correspondingly to said first to ninth pins of the peripheral port;

a cable including a plurality of wires connecting ones of the terminal pins of said plug connector with a printed circuit board of said peripheral device;

means for supplying a data signal including data representing a communication mode of said peripheral device on said second, third, seventh and eighth pins in response to a control signal supplied via said fourth and fifth pins from said apparatus;

means for short-circuiting said second pin with said first pin of said plug connector;

means for short-circuiting said sixth to eighth pins with said ninth pin of said plug connector; and

means for supplying a serial data signal to the apparatus via said third pin of said plug connector in synchronism with a clock signal supplied via the fifth pin while receiving a signal for selecting the peripheral device via the fourth pin.

5. A peripheral device for use with a data processing apparatus having an interface means with a peripheral port for communicating with a peripheral device with any of communication modes of a clocked parallel type, a clocked serial type, a three-wire handshake type and a TH/TR selection type, comprising:

a plug connector detachably connectable to said peripheral port, said plug connector having a set of terminal pins including first to ninth pins disposed in a row, said first pin for conducting one of a power source and ground potential, said ninth pin for conducting the other of the power source and the ground potential, said second, third, seventh and eighth pins for conducting data signals, said fourth and fifth pins for receiving control signals;

a cable including a plurality of wires connecting the terminal pins of said plug connector with terminals on a printed circuit board of said peripheral device;

means for supplying a data signal including identification data representing a communication mode of said peripheral device to the apparatus on said second, third, seventh and eighth pins in response to a control signal supplied from said apparatus for collecting the identification data via the fourth and fifth pins; and

means for supplying said apparatus with a data signal including manipulation data via at least one of said second, third, seventh and eighth pins in response to a second control signal supplied from said apparatus via at least one of said fourth and fifth pins.

6. A peripheral device for use with a data processing apparatus, said apparatus having a peripheral port with a set of terminal pins consisting of first to ninth pins disposed in a row, said first pin for conducting one of a power source and ground potential, said ninth pin for conducting the other of the power source and the ground potential, said second, third, seventh and eighth pins for conducting data signals, said fourth and fifth pins for conducting control signals, said

apparatus having an interface means for communicating with said peripheral device with any of communication modes of a clocked parallel type, a clocked serial type, a three-wire handshake type and a TH/TR selection type and for determining which one of the communication modes to use for communicating with said peripheral device connected to the peripheral port based on the data signals received on said second, third, seventh and eighth pins, said peripheral device comprising:

a plug connector detachably connectable to said peripheral port, said plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row correspondingly to said first to ninth pins of the peripheral port;

a cable including a plurality of wires connecting ones of the terminal pins of said plug connector with a printed circuit board of said peripheral device;

means for supplying a data signal including identification data representing the communication mode of said peripheral device on said second, third, seventh and eighth pins in response to a first control signal supplied from said apparatus for requesting the identification data via the fourth and fifth pins; and

means for supplying said apparatus with a data signal including manipulation data via at least one of said second, third, seventh and eighth pins in response to a second control signal supplied from said apparatus via at least one of said fourth and fifth pins.

12. A peripheral device for use with a data processing apparatus having an interface means for communicating with a peripheral device with any of communication modes of a clocked parallel type, a clocked serial type, a three-wire handshake type and a TH/TR selection type, said interface means including a socket connector with nine socket pins, comprising:

a plug connector detachably connectable to said socket connector, said plug connector having nine plug pins disposed correspondingly to the socket pins, said plug pins including a pair of first pins for connecting to fixed potentials, four second pins for conducting data signals, a pair of third pins for receiving control signals and a fourth pin which is disposed adjacent to one of said pair of third pins;

a cable including a plurality of wires connecting the plug pins of said plug connector with terminals on a printed circuit board of said peripheral device;

means for short-circuiting said fourth pin with one of said pair of third pins adjacently disposed to said fourth pin;

means for supplying a data signal including identification data representing a clocked parallel communication mode of said peripheral device on said second pins in response to a first control signal for requesting the identification data from said apparatus to said peripheral device via said pair of third pins; and

means for supplying said apparatus with a parallel data signal including manipulation data via said four second pins in response to a second control signal supplied from said apparatus via said pair of third pins.

13. A peripheral device for use with a data processing apparatus having a socket connector with nine socket pins, comprising:

a plug connector detachably connectable to said socket connector, said plug connector having nine plug pins disposed correspondingly to the socket pins, said plug pins including a pair of first pins for connecting to fixed potentials, four second pins for conducting data signals, a pair of third pins for receiving a control signal and a fourth pin which is disposed adjacent to one of said pair of

third pins;

a cable including a plurality of wires connecting the plug pins of said plug connector with terminals on a printed circuit board of said peripheral device;

short-circuiting means for short-circuiting said fourth pin with one of said pair of third pins within said plug connector; and

means for providing data signals including identification data representing a clocked parallel communication mode of said peripheral device on said second pins in response to the control signal for collecting the identification data from said apparatus to said peripheral device via said third pins.

15. A peripheral device for use with a data processing apparatus having an interface means for communicating with a peripheral device with any of communication modes of a clocked parallel type, a clocked serial type, a three-wire handshake type and a TH/TR selection type, said interface means including a socket connector with nine socket pins, comprising:

a plug connector detachably connectable to said socket connector, said plug connector having nine plug pins disposed correspondingly to the socket pins, said plug pins including a pair of first pins for connecting to fixed potentials, a plurality of second pins for conducting data signals, and two third pins for conducting control signals;

a cable including a plurality of wires connecting the plug pins of said plug connector with terminals on a printed circuit board of said peripheral device;

means for short-circuiting remaining plug pins other than said first pins, one of said plurality of second pins and said two third pins to at least one of said first pins; and

means for supplying a data signal including identification data representing a communication mode of said peripheral device on said plurality of second pins in response to a first control signal for requesting the identification data from said apparatus to said peripheral device via said third pins; and

means for supplying said apparatus with a serial data signal including manipulation data via said one second pin not short-circuited by said short-circuiting means in response to a second control signal supplied via said pair of third pins from said apparatus.

16. A peripheral device for use with a data processing apparatus having a socket connector with nine socket pins, comprising:

a plug connector detachably connectable to said socket connector, said plug connector having nine plug pins disposed correspondingly to the socket pins, said plug pins including a pair of first pins for connecting to fixed potentials, a plurality of second pins for conducting data signals, and two third pins for conducting control signals;

a cable including a plurality of wires connecting the plug pins of said plug connector with terminals on a printed circuit board of said peripheral device;

short-circuiting means for short-circuiting remaining plug pins other than said first pins, one of said plurality of second pins and said two third pins to at least one of said first pins in said plug connector; and

means for supplying a data signal including identification data representing a communication mode of said peripheral device on said plurality of second pins in

response to a control signal for requesting identification data from said apparatus to said peripheral device via said third pins.

18. A game apparatus, comprising:

a data processing apparatus having an interface means for communicating with a peripheral device with any of communication modes of a clocked parallel type, a clocked serial type, a three-wire handshake type and a TH/TR selection type, said interface means having a peripheral port with a plurality of terminal pins disposed in a row, said plurality of terminal pins in said row including a pair of first pins, one of said first pins for conducting one of a power source and ground potential and the other of said first pins for conducting the other of the power source and the ground potential, a plurality of second pins for conducting data signals, a pair of third pins for conducting control signals, said data processing apparatus further having means of determining which one of the communication modes to use based on the data signals on said plurality of second pins, means for conducting a first control signal for requesting identification data via said pair of third pins and a second control signal including a signal for selecting a peripheral device via one of said pair of third pins, and means for communicating in the determined communication mode; and

a peripheral device having a plug connector detachably connectable to said peripheral port, said plug connector having a plurality of plug pins identical in number and disposed in a row in correspondence to the terminal pins of said peripheral port, said peripheral device further having a cable including a plurality of wires connecting the plug pins of said plug connector with a printed circuit board of said peripheral device and means for supplying the data signals including identification data representing the communication mode of said peripheral device on said plurality of second pins in response to the first control signal supplied from said apparatus, and

means for supplying said data processing apparatus with a data signal including manipulation data via at least one of said plurality of second pins in response to the second control signal supplied from said apparatus.

24. A game apparatus, comprising:

a data processing apparatus having a peripheral port with a plurality of terminal pins disposed in a row, said plurality of terminal pins in said row including a pair of first pins, one of said first pins for conducting one of a power source and ground potential and the other of said first pins for conducting the other of the power source and the ground potential, four second pins for conducting data signals, three third pins, said second and third pins being disposed between said pair of first pins, said data processing apparatus further having means for determining a communication mode based on the data signals on said four second pins, means for conducting a control signal for requesting identification data via at least one of said third pins, and means for communication in the determined communication mode; and

a peripheral device having a plug connector detachably connectable to said peripheral port, said plug connector having a plurality of plug pins identical in number and disposed in a row in correspondence to the terminal pins of said peripheral port, said peripheral device further having a cable including a plurality of wires connecting the plug pins with a printed circuit board of said peripheral device and means for supplying data signals including identification data representing the communication mode of said peripheral device on said four second pins in response to the control signal supplied from said apparatus,

said data processing apparatus further comprising means for transmitting a signal for selecting said peripheral device via one of said third pins in the peripheral

port and a clock signal via another of said third pins, and

said peripheral device further comprising means for transmitting serial data signals via one of the second pins to said apparatus and means for selectively short-circuiting a remaining one of the third pins and a remaining three of the second pins with said first pins.

42. A peripheral device for use with a data processing apparatus having a peripheral port, means for supplying a power source potential, a ground potential, and a control signal through said peripheral port, and an interface means for communicating with a peripheral device with a communication mode of any a clocked parallel type, a clocked serial type, a three-wire handshake type or a TH/TR selection type and for determining which one of the communication modes to use for communicating with a peripheral device connected to the peripheral port based on data signals supplied from the peripheral device, the peripheral device comprising:

a connector detachably connectable to said peripheral port, said connector having a set of terminal contacts including first to ninth contacts disposed in a row, said first contact for connecting to one of the power source potential and the ground potential, said ninth contact for connecting to the other of the power source potential and the ground potential, said second, third, seventh and eighth contacts for transmitting data signals, and said fourth and fifth contacts for receiving the control signal;

a cable including a plurality of wires connecting ones of the terminal contacts of said connector with a printed circuit board of said peripheral device;

means, when said peripheral device is activated by the power source potential and the ground potential supplied through the peripheral port, for supplying a data signal including identification data representing a communication mode of said peripheral device on said second, third, seventh and eighth contacts in response to a first control signal supplied from said apparatus for requesting the identification data; and

means for supplying said apparatus with a data signal including manipulation data via at least one of said second, third, seventh and eighth contacts in response to a second control signal supplied from said apparatus via at least one of said fourth and fifth contacts.

45. A peripheral device for use with a data processing apparatus having a peripheral port and means for supplying a power source potential, a ground potential, and a control signal through said peripheral port, comprising:

a connector detachably connectable to said peripheral port, said connector having a set of terminal contacts including first to ninth contacts disposed in a row, said first contact for connecting to one of the power source potential and the ground potential, said ninth contact for connecting to the other of the power source potential and the ground potential, said second, third, seventh and eighth contacts for conducting data signals, and said fourth and fifth contacts for receiving the control signal;

a cable including a plurality of wires connecting ones of the terminal contacts of said connector with a printed circuit board of said peripheral device;

means for supplying data signals including identification data representing a communication mode of said peripheral device on said second, third, seventh and eighth contacts in response to a control signal supplied from said apparatus for requesting the identification data; and

means for short-circuiting selected ones of said contacts.

49. A peripheral device for use with a data processing apparatus having a peripheral port and means for supplying a power source potential, a ground potential, and a control signal through said peripheral port, comprising:

a connector detachably connectable to said peripheral port, said connector having a set of terminal contacts including first to ninth contacts disposed in a row, said first contact for connecting to one of the power source potential and the ground potential, said ninth contact for connecting to the other of the power source potential and the ground potential, said second, third, seventh and eighth contacts for conducting data signals, and said fourth and fifth contacts for receiving the control signal;

a cable including a plurality of wires connecting ones of the terminal contacts of said connector with a printed circuit board of said peripheral device, the wires of said cable being fewer in number than said terminal contacts; and

means for supplying the data signals including identification data representing a communication mode of said peripheral device to the apparatus via said second, third, seventh and eighth contacts in response to a control signal supplied from said apparatus for requesting the identification data.

50. A peripheral device for use with a data processing apparatus having a peripheral port and means for supplying a power source potential, a ground potential, and a control signal through said peripheral port, comprising:

a connector detachably connectable to said peripheral port, said connector having a set of terminal contacts including first to ninth contacts disposed in a row, said first contact for connecting to one of the power source potential and the ground potential, said ninth contact for connecting to the other of the power source potential and the ground potential, said second, third, seventh, and eighth contacts for conducting data signals, and said fourth and fifth contacts for receiving the control signal;

a cable including a plurality of wires connecting ones of the terminal contacts of said connector with a printed circuit board of said peripheral device; and

means for supplying the data processing apparatus with data signals including identification data representing a three-wire handshake type communication mode, including means, in response to a control signal of "1" to the fourth contact and "1" to the fifth contact and a control signal of "0" to the fourth contact and "1" to the fifth contact supplied from the data processing apparatus, for supplying a data signal of "0" to the seventh contact, "0" to the eighth contact, "0" to the second contact and "1" to the third contact, respectively, wherein "1" and "0" correspond to the power source and ground potentials, respectively, so that the data processing apparatus determines that the peripheral device employs the three-wire handshake type communication mode.

51. A peripheral device for use with a data processing apparatus having a peripheral port, and means for supplying a power source potential, a ground potential, and a control signal through said peripheral port, comprising:

a connector detachably connectable to said peripheral port, said connector having a set of terminal contacts including first to ninth contacts disposed in a row, said first contact for connecting to one of the power source potential and the ground potential, said ninth contact for connecting to the other of the power source potential and the ground potential, said second, third, seventh and eighth contacts for conducting data signals, and said fourth and fifth contacts for receiving the control signal;

a cable including a plurality of wires connecting ones of the terminal contacts of said connector with a printed circuit board of said peripheral device; and

means for supplying the data processing apparatus with the data signals indicative of a three-wire handshake type communication mode, including means for supplying a data signal of "0" to the seventh, the eighth and the second contacts, respectively, and "1" to the third contact in response to the control signal from the data processing apparatus, wherein "1" and "0" correspond to the power source and ground potentials, respectively, so that the data processing apparatus determines that the peripheral device employs the three-wire handshake type communication mode.

52. A peripheral device for use with a data processing apparatus having a peripheral port, and means for supplying a power source potential, a ground potential, and a control signal through said peripheral port, comprising:

a connector detachably connectable to said peripheral port, said connector having a set of terminal contacts including first to ninth contacts disposed in a row, said first contact for connecting to one of the power source potential and the ground potential, said ninth contact for connecting to the other of the power source potential and the ground potential, said second, third, seventh and eighth contacts for conducting data signals, and said fourth and fifth contacts for receiving the control signal;

a cable including a plurality of wires connecting ones of the terminal contacts of said connector with a printed circuit board of said peripheral device;

means for supplying the fifth contact and the sixth contact with the same potential; and

means for supplying the data processing apparatus with the data signals indicative of a clocked parallel type communication mode, including means for supplying a data signal of "0" to the seventh contact, a data signal of "0" to the eighth contact, a data signal of "1" to the second contact and "1" to the third contact in response to the control signal from the data processing apparatus, wherein "1" and "0" correspond to the power source and ground potentials, respectively, so that the data processing apparatus determines that the peripheral device employs the clocked parallel type communication mode.

54. A peripheral device for use with a data processing apparatus having a peripheral port, and means for supplying a power source potential, a ground potential, and control signals through said peripheral port, comprising:

a connector detachably connectable to said peripheral port, said connector having a set of terminal contacts including first to ninth contacts disposed in a row, said first contact for connecting to one of the power source potential and the ground potential, said ninth contact for connecting to the other of the power source potential and the ground potential, said third contact for transmitting data signals and said fourth and fifth contacts for receiving the control signal;

a cable including a plurality of wires connecting ones of the terminal contacts of said connector with a printed circuit board of said peripheral device;

a plurality of key switches disposed on the peripheral device;

means for supplying the data processing apparatus with data signals indicative of a clocked serial type communication mode, including means for supplying the second contact with the same signal potential as that of the first contact so as to supply a data signal of "1" to the second contact, means for supplying the sixth, the

seventh and eighth contacts with the same signal potential as that of the ninth contact so as to supply a data signal of "0" to the sixth, seventh and eighth contacts, respectively, and means for supplying a data signal of "0" to the third contact in response to a control signal from the data processing apparatus, wherein "1" and "0" correspond to the power source and ground potentials, respectively, so that the data processing apparatus determines that the peripheral device employs the clocked serial type communication mode; and

means for supplying the apparatus with clocked serial data including data indicative of the key switches in response to a peripheral device selection signal supplied via said fourth contact and the clock signal supplied via said fifth contact.

56. A peripheral device for use with a data processing apparatus having a peripheral port, means for supplying a power source potential, a ground potential, and a control signal through said peripheral port, the peripheral device comprising:

a connector detachably connectable to said peripheral port, said connector having a set of terminal contacts including first to ninth contacts disposed in a row, said first contact for connecting to one of the power source potential and the ground potential, said ninth contact for connecting to the other of the power source potential and the ground potential;

a cable including a plurality of wires connecting ones of the terminal contacts of said connector with a printed circuit board of said peripheral device; and

means for supplying data signals of a predetermined data combination to the apparatus via said second, third, seventh and eighth contacts in response to receipt from said data processing apparatus of the control signal in a first signal combination in which the fourth contact conducts "1" and the fifth contact conducts "1", and in a second signal combination in which the fourth contact conducts "0" and the fifth contact conducts "1", wherein "1" and "0" correspond to the power source and ground potentials, respectively, said data signal of the predetermined data combination being selected so as to comply with the following formulas:

{(data R in TH="1") or (data L in TH="1")}.times.8h+{(data D in TH="1") or (data U in TH="1")}.times.4h+{(data R in TH="0") or (data L in TH="0")}.times.2h+{(data D in TH="0") or (data U in TH="0")}.times.1h=Bh

wherein the data R is a data supplied on the seventh pin, the data L on the eighth pin, data D on the second pin and the data U on the third pin, and TH is the control signal in said first or second signal combination supplied on the fourth pin,

thereby enabling the data processing apparatus to determine a TH/TR communication mode based upon the data from the seventh contact, the eighth contact, the second contact, and the third contact.

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L3: Entry 13 of 20 File: USPT May 13, 1997

US-PAT-NO: 5630170
DOCUMENT-IDENTIFIER: US 5630170 A

TITLE: System and method for determining peripheral's communication mode over row of pins disposed in a socket connector

DATE-ISSUED: May 13, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Koizumi; Masahiro	Tokyo			JP
Niizuma; Naoki	Tokyo			JP
Kawase; Yasuhisa	Tokyo			JP
Ikebe; Hajime	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Kabushiki Kaisha SEGA Enterprises	Tokyo			JP	03

APPL-NO: 08/ 445108 [PALM]
DATE FILED: May 19, 1995

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	6-246581	October 12, 1994

INT-CL: [06] G06 F 3/00, G06 F 3/023, G06 F 13/38

US-CL-ISSUED: 395/834; 395/893, 463/36, 463/40
US-CL-CURRENT: 710/12; 366/129, 463/36, 463/40, 710/73

FIELD-OF-SEARCH: 439/43, 439/189, 439/604, 439/45, 439/44, 439/46, 439/47, 439/49, 439/79, 439/95, 439/119, 439/221, 439/362, 439/369, 439/133, 395/834, 395/835, 395/831, 395/836, 395/893, 273/143B, 463/36, 463/37, 463/38, 463/40, 345/161, 345/168

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4484266	November 1984	Becker et al.	364/200

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☐	4501424	February 1985	Stone et al.	273/143B
☐	4592012	May 1986	Braun	364/900
☐	4888680	December 1989	Sander et al.	364/200
☐	4972470	November 1990	Farago	380/3
☐	5151985	September 1992	Sander et al.	395/500
☐	5175820	December 1992	Gephardt	395/834
☐	5179710	January 1993	Coschieri	395/750
☐	5207426	May 1993	Inoue et al.	273/148B
☐	5274766	December 1993	Long et al.	595/834
☐	5375210	December 1994	Monnes et al.	595/830
☐	5379382	January 1995	Work et al.	395/275

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
60-27566	February 1985	JP	
63-118928	May 1988	JP	
63-118830	May 1988	JP	
2-62618	March 1990	JP	
9110715	November 1992	GB	
WO-A-8809573	December 1988	WO	
WO-A-9416774	August 1994	WO	
WO95/01630	January 1995	WO	
WO95/01609	January 1995	WO	
WO95/01629	January 1995	WO	

OTHER PUBLICATIONS

Patent Abstracts of Japan, vol. 14, No. 240, p. 151, May 22, 1990 (Abstract of JP 2-062618).

ART-UNIT: 237

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Dinh; D.

ATTY-AGENT-FIRM: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

ABSTRACT:

A peripheral device for use with a data processing apparatus. The apparatus has a peripheral port with a set of terminal pins consisting of first to ninth pins disposed in a row. The first pin is assigned for one of a power source and the ground potential, the ninth pin for the other of the power source and the ground potential, the second, third, seventh and eighth pins for transmitting data

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signals, and the fourth to sixth pins for transmitting control signals. The apparatus has an element for selecting the communication mode of the peripheral device connected to the peripheral port, based on the data signals transmitted from the second, third, seventh and eighth pins. The peripheral device comprises a plug connector detachably connected to the peripheral port, the plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row, a cable including a plurality of wires connecting the terminal pins of the plug connector with terminals on an internal printed circuit board, and an element for transmitting data signals including identification data representing the communication mode via at least one of the second, third, seventh and eighth pins in synchronization with a clock signal supplied from the apparatus.

61 Claims, 19 Drawing figures

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L1: Entry 1 of 4 File: USPT Aug 17, 1999

US-PAT-NO: 5938754
DOCUMENT-IDENTIFIER: US 5938754 A

TITLE: Fieldbus connector including dual connectors

DATE-ISSUED: August 17, 1999

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 710/129; 714/27
US-CL-CURRENT: 710/305; 714/27

FIELD-OF-SEARCH: 395/183.03, 395/183.21, 395/200.54, 395/280, 395/306, 395/309, 439/255, 714/27, 714/45, 710/100, 710/126, 710/129, 709/224

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L1: Entry 2 of 4 File: USPT May 18, 1999

US-PAT-NO: 5905249
DOCUMENT-IDENTIFIER: US 5905249 A

TITLE: Multiple-interface selection system for computer peripherals

DATE-ISSUED: May 18, 1999

INT-CL: [06] G06 K 7/10

US-CL-ISSUED: 235/462.15; 235/462.13, 235/462.43
US-CL-CURRENT: 235/462.15; 235/462.13, 235/462.43

FIELD-OF-SEARCH: 235/462, 235/472, 235/462.15, 235/462.13, 235/462.43, 235/462.45, 235/462.47, 439/502, 439/620

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L1: Entry 3 of 4 File: USPT Dec 9, 1997

US-PAT-NO: 5696988
DOCUMENT-IDENTIFIER: US 5696988 A

TITLE: Current/voltage configurable I/O module having two D/A converters serially coupled together such that data stream flows through the first D/A to the second D/A

DATE-ISSUED: December 9, 1997

INT-CL: [06] G06 F 13/12

US-CL-ISSUED: 395/821; 395/824, 341/144, 341/139
US-CL-CURRENT: 710/1; 341/139, 341/144, 710/4

FIELD-OF-SEARCH: 340/347, 341/145, 341/139, 341/144, 364/900, 360/31, 324/248, 395/821, 395/824

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L1: Entry 4 of 4 File: USPT Jan 21, 1997

US-PAT-NO: 5596169
DOCUMENT-IDENTIFIER: US 5596169 A

TITLE: Combined SCSI/parallel port cable

DATE-ISSUED: January 21, 1997

INT-CL: [06] H01 B 11/02

US-CL-ISSUED: 174/33; 174/34, 341/89, 439/505
US-CL-CURRENT: 174/33; 174/34, 341/89, 439/502, 439/505

FIELD-OF-SEARCH: 174/33, 174/27, 174/32, 174/34, 361/686, 439/65, 341/89, 341/100, 341/101

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